Universidad Politécnica de Valencia

Escuela Técnica Superior de Ingeniería del Diseño

Grado en Ingeniería Electrónica Industrial y Automática

Trabajo de Fin de Grado

DISEÑO E IMPLEMENTACIÓN DE UN RECTIFICADOR TRIFÁSICO TOTALMENTE CONTROLADO PARA EL CONTROL DE UN MOTOR DC

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I MEMORIA

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5 INTRODUCCIÓN

En ingeniería se conoce como tensión eléctrica a la magnitud física que cuantifica la diferencia de potencial eléctrico entre dos puntos. Cuando se unen dos puntos mediante un elemento conductor entre los cuales existe una diferencia de potencial se produce el fenómeno conocido como corriente eléctrica.

Existen dos tipos de corriente: corriente continua (CC) y corriente alterna (CA). La diferencia fundamental entre la corriente continua y la corriente alterna es que esta última varía con el tiempo repitiéndose de forma periódica, la más usada es la corriente alterna sinusoidal. El uso de corriente alterna sinusoidal tiene ciertas ventajas sobre la corriente continua ya que es más eficiente a la hora de generar, transportar y distribuirla. Dado que la mayoría de los dispositivos eléctricos y electrónicos funcionan con corriente continua existe una necesidad de transformar esa corriente alterna a corriente continua. Para cubrir dicha necesidad se hace uso de los convertidores ca/cc, más comúnmente conocidos como rectificadores.

Los rectificadores hacen uso de interruptores electrónicos que se caracterizan por tener dos estados conduciendo y no conduciendo, esto idealmente corresponde con un cortocircuito y circuito abierto respectivamente. Los dispositivos más comunes y sencillos para estas aplicaciones son los diodos, pero estos no permiten tener control sobre retraso o ángulo de disparo de los mismos, para ello existen otros interruptores electrónicos más complejos conocidos como tiristores.

En este trabajo se realizará un modelado de un convertidor ca/cc trifásico de onda completa totalmente controlado por medio de tiristores para poner en funcionamiento un motor de corriente continua además de un control PI para la regulación de velocidad en bucle cerrado. La necesidad de implementar un regulador viene dada a la inestabilidad de funcionamiento del motor en bucle abierto.

6 CONCEPTOS PREVIOS Y FUNDAMENTO TEÓRICO

6.1 Corriente alterna y corriente continua

La corriente continua es aquella no varía con el tiempo, es decir, el flujo de corriente es constante entre dos puntos con diferente potencial (**Fig. 1**). Se caracteriza principalmente por su valor de tensión (V) y de corriente (I).

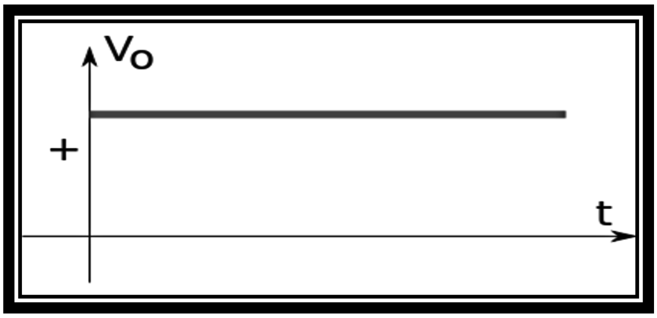

Fig. 1 Representación gráfica de la tensión frente al tiempo en CC

Por otro lado, la corriente alterna es aquella que varía con el tiempo y se repite de forma periódica (**Fig. 2**)Los parámetros que caracterizan la corriente alterna son:

1. **Amplitud**: valor de tensión o corriente instantáneos (V(t), I(t))
2. **Período**: duración temporal de cada ciclo (T)
3. **Frecuencia**: número de ciclos por segundo (f = 1/T)
4. **Pulsación**: se define como ω = 2πf
5. **Fase**: desplazamiento angular de la señal respecto del origen de ángulos (φ).

Además, se emplean otros valores para cuantificar tensiones y corrientes que son:

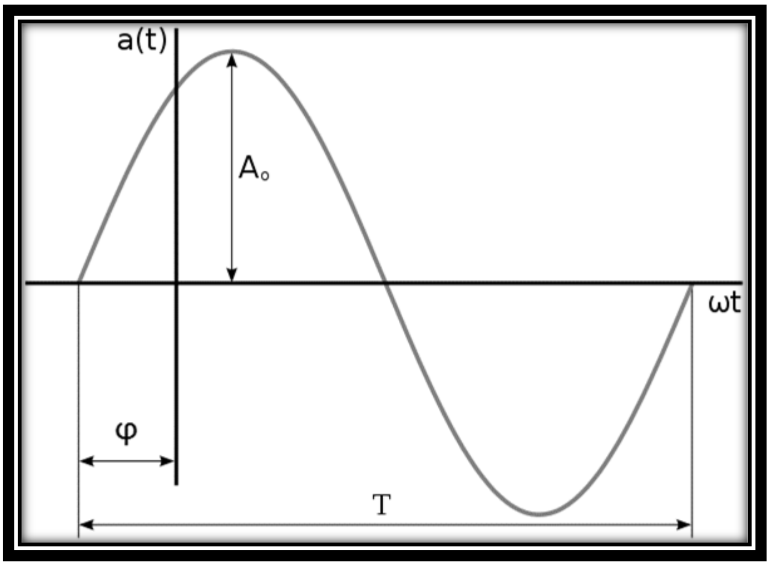

__Fig. 2__ Representación gráfica de una señal sinusoidal y sus parámetros

1. **Valor medio**: media aritmética de los valores instantáneos durante un periodo ya sea de tensión (**1**) o de corriente (**2**).

$$V_{med} = \frac{1}{T}\int_0^T V^2(t)dt \tag{1}$$

$$I_{med} = \frac{1}{T}\int_0^T I^2(t)dt \tag{2}$$

2. **Valor instantáneo**: valor de la tensión (**3**) o corriente (**4**) en función del tiempo.

$$V(t) = V_o \cdot sen(\omega t + \varphi) \tag{3}$$

$$I(t) = I_o \cdot sen(\omega t + \varphi) \tag{4}$$

3. **Valor eficaz**: media cuadrática de los valores instantáneos de tensión (**5**) o corriente (**6**) durante un periodo.

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2(t)dt} \tag{5}$$

$$I_{rms} = \sqrt{\frac{1}{T}\int_0^T I^2(t)dt} \tag{6}$$

4. **Valor máximo**: amplitud de la onda senoidal desde el eje de abscisas ya sea tensión (**7**) o corriente (**8**).

$$V_m = \sqrt{2} \cdot V_{rms} \tag{7}$$

$$I_m = \sqrt{2} \cdot I_{rms} \tag{8}$$

6.2 Tiristor y SCR

Los tiristores son interruptores electrónicos utilizados en los circuitos electrónicos de potencia donde es necesario controlar la activación del interruptor. Los tiristores cuentan con tres terminales y dentro de la familia se encuentran: el rectificador controlado de silicio (SCR), el triac, el tiristor de bloqueo por puerta (GTO) y el tiristor MCT o tiristor controlado por MOS (metal-óxido-semiconductor). Los tres terminales son el ánodo (A), el cátodo (K) y la puerta (G).

En el ámbito cuotidiano suelen emplearse los términos SCR y tiristor como sinónimos. Una de las características de los tiristores es que pueden soportar altas corrientes y altas tensiones de bloqueo, pero las frecuencias de conmutación están limitadas a valores de entre 10 y 20kHz, aproximadamente.

Para que el SCR (**Fig. 3**) entre en conducción, hay que aplicar una corriente de puerta cuando la tensión ánodo-cátodo sea positiva. Una vez que el dispositivo haya entrado en conducción, la señal de la puerta deja de ser necesaria para mantener la corriente de ánodo. El SCR continuará conduciendo mientras la corriente de ánodo siga siendo positiva y esté por encima de un valor mínimo denominado nivel de mantenimiento.

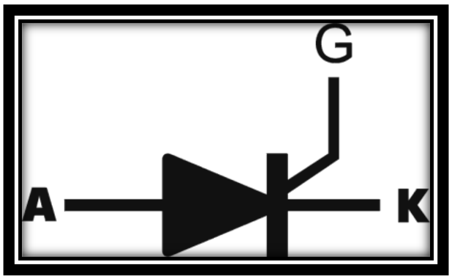

Fig. 3 *Modelo de SCR y sus terminales*

6.3 Transformadores

Para poder trabajar con el motor hay que adecuar las tensiones a los valores aceptados por el dispositivo. Así mismo para la alimentación de la etapa de control también es necesario un nivel de tensión adecuado para el correcto funcionamiento de los dispositivos. Otra característica de suma importancia es la capacidad de aislamiento eléctrico, esto nos permitirá tener los puntos de referencia de cada subcircuito aislados.

La relación entre la fuerza electromotriz inductora (Ep), la aplicada al devanado primario y la fuerza electromotriz inducida (Es), la obtenida en el secundario, es directamente proporcional al número de espiras de los devanados primario (Np) y secundario (Ns). La relación de transformación (m) indica el aumento o decremento que sufre el valor de la tensión de salida con respecto a la tensión de entrada, es decir, la relación entre la tensión de salida y la de entrada (**9**).

$$m = \frac{Ep}{Es} = \frac{Vp}{Vs} = \frac{Np}{Ns} \qquad (\mathbf{9})$$

6.4 TCA785

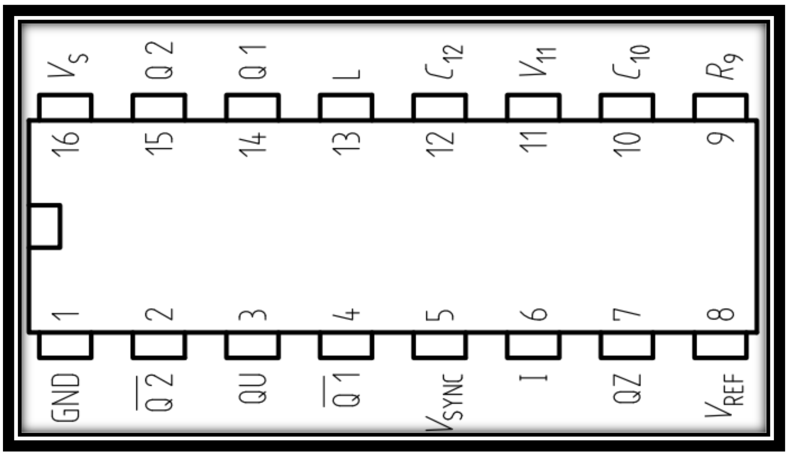

Fig. 4 *Patillaje del circuito integrado TCA785*

El circuito integrado TCA785 (**Fig. 4**) (Tabla 1) está enfocado a aplicaciones de control de fase para tiristores, triacs y transistores principalmente. Los pulsos de disparo pueden regularse desde 0 hasta 180 grados. Las aplicaciones típicas incluyen circuitos convertidores, reguladores de AC y controles de corriente trifásicos.

Tabla 1 *Número de pin, símbolo y descripción del patillaje del CI TCA785.*

PIN	Símbolo	Función
1	GND	Masa
2	Q2	Salida 2 invertida
3	QU	Salida U
4	Q1	Salida 1 invertida
5	Vsync	Tensión de sincronización
6	I	Inhibición
7	QZ	Salida Z
8	Vref	Tensión estabilizada
9	R9	Resistencia de rampa
10	C10	Condensador de rampa
11	V11	Tensión de control
12	C12	Extensión de pulso
13	L	Pulso largo
14	Q1	Salida 1
15	Q2	Salida 2
16	Vs	Tensión de alimentación

6.4.1 Principio de funcionamiento

La señal de sincronización se obtiene a través de una impedancia de alto valor conectada al terminal 5. Tras esto, un detector de pasos por cero se encarga de detectarlos y enviarlos al registro de sincronización.

Este registro de sincronización controla un generador de rampa, el condensador C10 se carga por una corriente constante (determinada por R9). Si el voltaje V10 rampa excede la tensión de control V11 (ϕ ángulo de disparo), una señal es procesada a la unidad lógica. Dependiendo del valor de la V11, el ángulo ϕ desencadenante puede ser desplazado dentro de un ángulo de fase de 0˚ a 180˚. Para cada media onda, un pulso positivo de aprox. 30 us de duración aparece en las salidas Q1 y Q2. La duración del pulso se puede prolongar hasta 180˚ a través de un condensador C12. Si el pin 12 está conectado a tierra, los pulsos tendrán una duración entre ϕ y 180˚.

Una señal de ϕ + 180˚ que puede ser utilizado para controlar una lógica externa, a través del pin 3. Una señal que corresponde al enlace NOR de Q 1 y Q 2 está disponible en la salida QZ (pin 7). La entrada de inhibición se puede utilizar para desactivar las salidas Q1, Q2 y sus respectivas negadas.

El Pin 13 se puede utilizar para ampliar longitud de pulso de las salidas negadas (180˚ - ϕ) (**Fig. 5**).

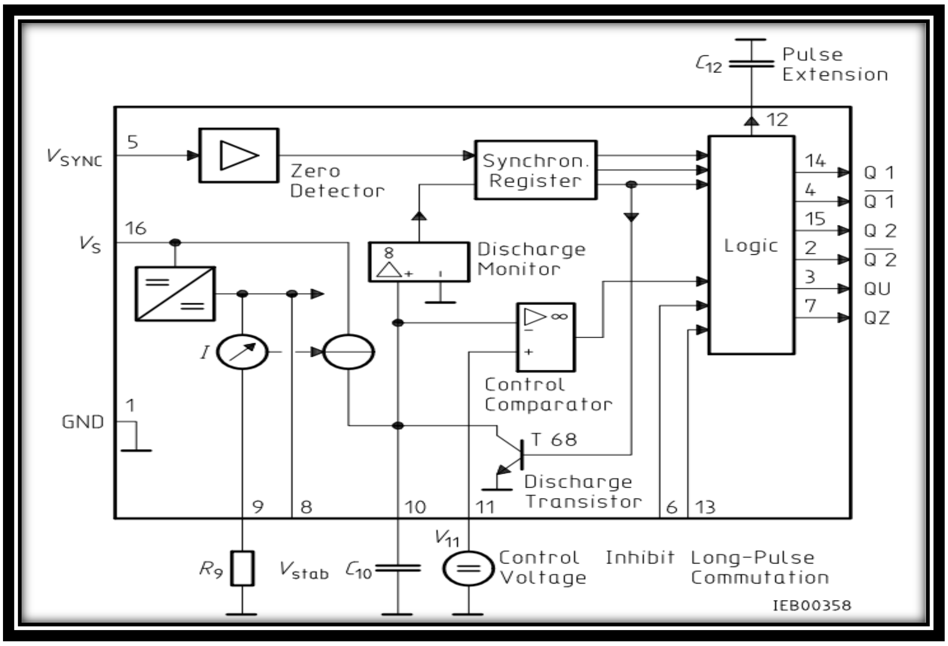

Fig. 5 Diagrama de bloques del TCA785

6.5 555

El circuito integrado 555 o, generalmente, 555 sirve generalmente para generar retardos de tiempo u oscilaciones precisas. Puede trabajar en diferentes configuraciones tales como: multivibrador monostable, astable, conformador y/o detector de pulsos. En este trabajo se hará uso de la configuración: multivibrador astable.

En la configuración multivibrador astable (**Fig. 6**) la entrada de RESET (patilla 4) se conecta a +Vcc para evitar puestas a cero accidentales de la salida. El condensador de la patilla 5 no es necesario, pero evita ruidos no deseados en la señal de salida. Por otro lado, R1, R2 y C1 conforman la constante de carga y R2 y C1 la de descarga.

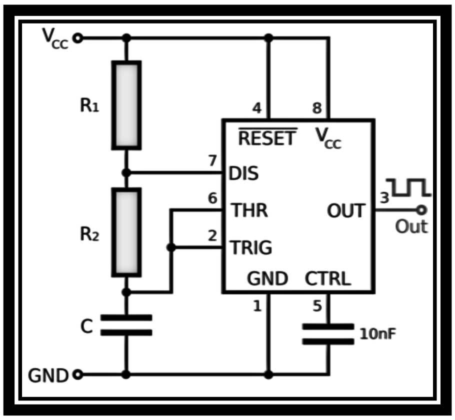

__Fig. 6__ Configuración del CI 555 en modo astable

Esta configuración se rige bajo varias ecuaciones que determinan el tiempo que la señal de salida estará a nivel alto y el tiempo que estará a nivel bajo. A consecuencia de esto tenemos la ecuación del periodo (**10**)) y de la frecuencia (**11**) de la señal de salida del integrado.

$$T = 0.693(R_1 + 2R_2)C_1 \; s \qquad (\mathbf{10})$$

$$F = \frac{1}{T} = \frac{1.44}{R_1 + 2R_2C_1} \; Hz \qquad (\mathbf{11})$$

7 RED TRIFÁSICA

Un sistema trifásico se caracteriza por contar con 3 fases entre la cuales existe un desfase. El sistema trifásico de tensiones senoidales a usar es equilibrado lo que implica que tanto la tensión o corriente eficaz, la pulsación y el desfase son iguales (**Fig. 7**).

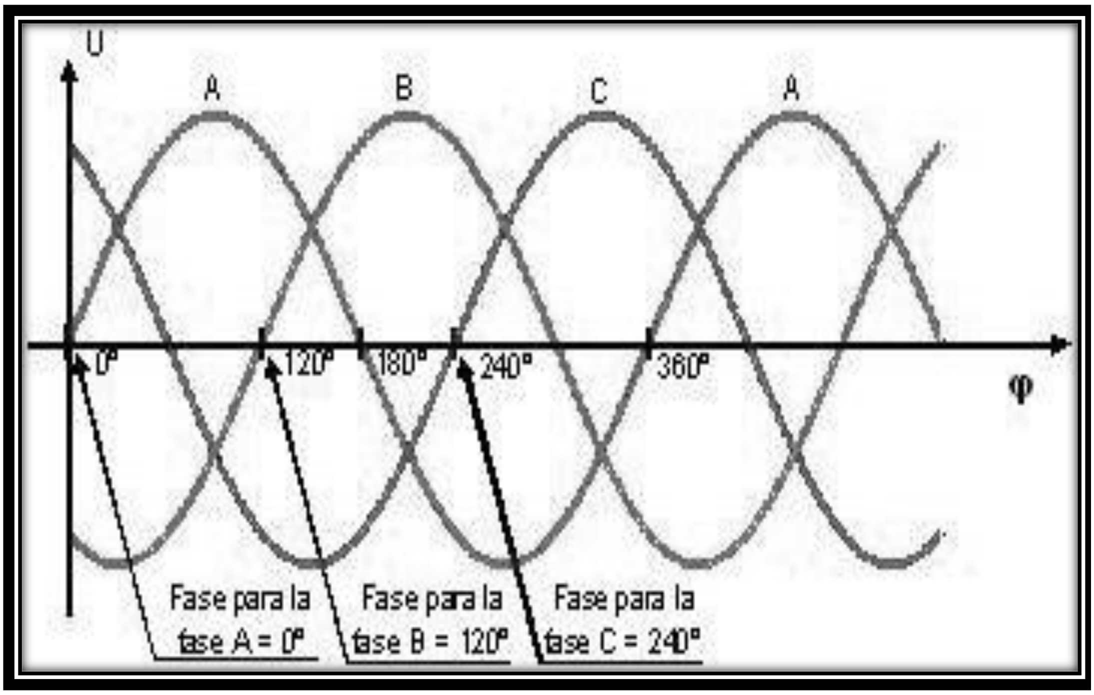

Fig. 7 *Representación gráfica del sistema de tensiones trifásico equilibrado*

Estas tensiones se conocen como tensiones simples o de fase. Los tres generadores contarán con un punto común que servirá de referencia a estas tensiones denominado Neutro (N). El sistema trifásico a usar contará con un desfase de 120° entre fases, 230 V_{RMS} por fase y 50 Hz de frecuencia. Analíticamente esto puede expresarse con las ecuaciones (**12**), (**13**) y (**14**)).

$$V_{an} = V_m \cdot \cos(\omega t) \qquad (\mathbf{12})$$

$$V_{bn} = V_m \cdot \cos\left(\omega t + \frac{2\pi}{3}\right) \qquad (\mathbf{13})$$

$$V_{cn} = V_m \cdot \cos\left(\omega t - \frac{2\pi}{3}\right) \qquad (\mathbf{14})$$

La tensión entre dos fases se conoce como tensión compuesta. Para este sistema el valor de dichas tensiones se obtiene con las ecuaciones (**15**), (**16**) y (**17**).

$$V_{ab} = V_{an} - V_{bn} = \sqrt{3} \cdot V_m \cdot sen\left(\omega t + \frac{\pi}{6}\right) \qquad (\mathbf{15})$$

$$V_{bc} = V_{bn} - V_{cn} = \sqrt{3} \cdot V_m \cdot sen\left(\omega t + \frac{\pi}{2}\right) \qquad (\mathbf{16})$$

$$V_{ca} = V_{cn} - V_{an} = \sqrt{3} \cdot V_m \cdot sen\left(\omega t - \frac{\pi}{2}\right) \qquad (\mathbf{17})$$

8 CONVERTIDORES CA/CC

8.1 Definición y generalidades

Los convertidores ca/cc o rectificadores permiten obtener un potencial a la salida de corriente continua a partir de una corriente alterna. Para llevar a cabo dicha conversión se hacen uso de conmutadores electrónicos como son los diodos, pero estos no permiten controlar el ángulo de disparo por lo que es necesario el uso de elementos más complejos como tiristores.

Los rectificadores que hacen uso de tiristores o de algún otro elemento que permita el control del ángulo de disparo se conocen como rectificadores controlados. También existen los conocidos como rectificadores semicontrolados en cuyo puente tienen una combinación de elementos controlados y no controlados de conmutación.

Convertidor ca/cc de "onda completa" es aquel con el cual se rectifica ambos semiciclos de la señal sinusoidal (**Fig. 8**)

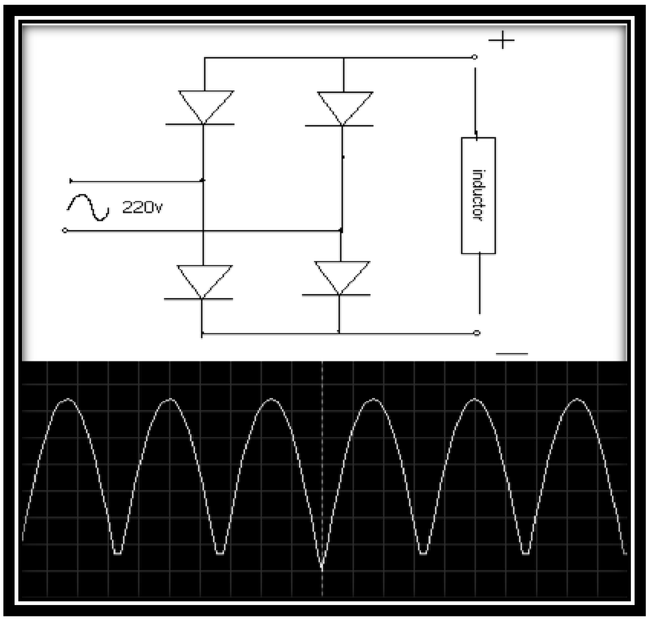

Fig. 8 *Rectificador monofásico de onda completa*

8.2 Rectificador trifásico totalmente controlado

El puente del convertidor ca/cc totalmente controlado de onda completa es aquel que cuenta con tiristores para llevar a cabo la rectificación de ambos semiciclos de la señal senoidal. De este modo se tiene control sobre el ángulo de disparo de cada tiristor permitiendo controlar la tensión y corriente de salida del rectificador (**Fig. 9**).

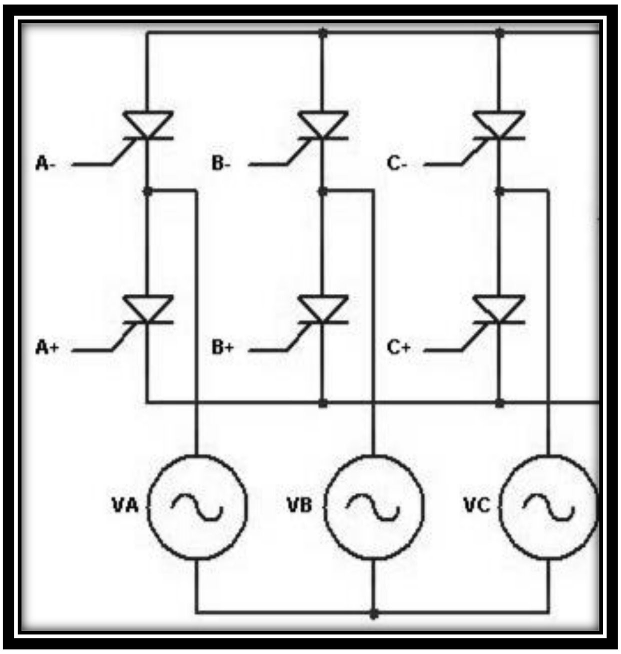

Fig. 9 Rectificador trifásico totalmente controlado

En ωt = π/6+α, el tiristor T5, ya conduce y el tiristor T1 se activa. Durante el intervalo (π/6 + α) ≤ ωt ≤ (π/2 + α) conducen los tiristores T1 y T5 y a través de la carga aparece el voltaje de línea a línea (vab = van - vbn). En ωt = π/2+α, el tiristor T6 se dispara y el tiristor T5 inmediatamente invierte su polaridad. El tiristor T5 se desactiva por conmutación natural. Durante el intervalo (π/2 + α) ≤ ωt ≤ (5π/6 + α), los tiristores T1 y T6 conducen y el voltaje de línea a línea, Vca, aparece a través de la carga., la secuencia de disparo es 16, 62, 24, 43, 35 y 51. En la figura 8 aparecen las formas de onda de tensión, para la tensión de salida, para la corriente de entrada y la corriente a través del tiristor (**Fig. 10**).

En estos rectificadores la tensión promedio de corriente continua (Vcc) se obtiene mediante la expersión (**18**).

$$V_{CC} = \frac{3}{\pi}\int_{\frac{\pi}{6}+\alpha}^{\frac{\pi}{2}+\alpha} \sqrt{3}\cdot V_m \cdot sen\left(\omega t+\frac{\pi}{6}\right)d(\omega t) = \frac{3\sqrt{3}\cdot V_m\cdot \cos(\alpha)}{\pi} \qquad (\mathbf{18})$$

El valor eficaz de la tensión de salida se calcula con la expresión (**19**).

$$V_{RMS} = \sqrt{\frac{3}{\pi}\int_{\frac{\pi}{6}+\alpha}^{\frac{\pi}{2}+\alpha}\left[\sqrt{3}\cdot V_m \cdot sen\left(\omega t + \frac{\pi}{6}\right)\right]^2 d(\omega t)} = \sqrt{3}V_m\sqrt{\frac{1}{2}+\frac{3\sqrt{3}}{4\pi}\cos(2\alpha)} \quad (\mathbf{19})$$

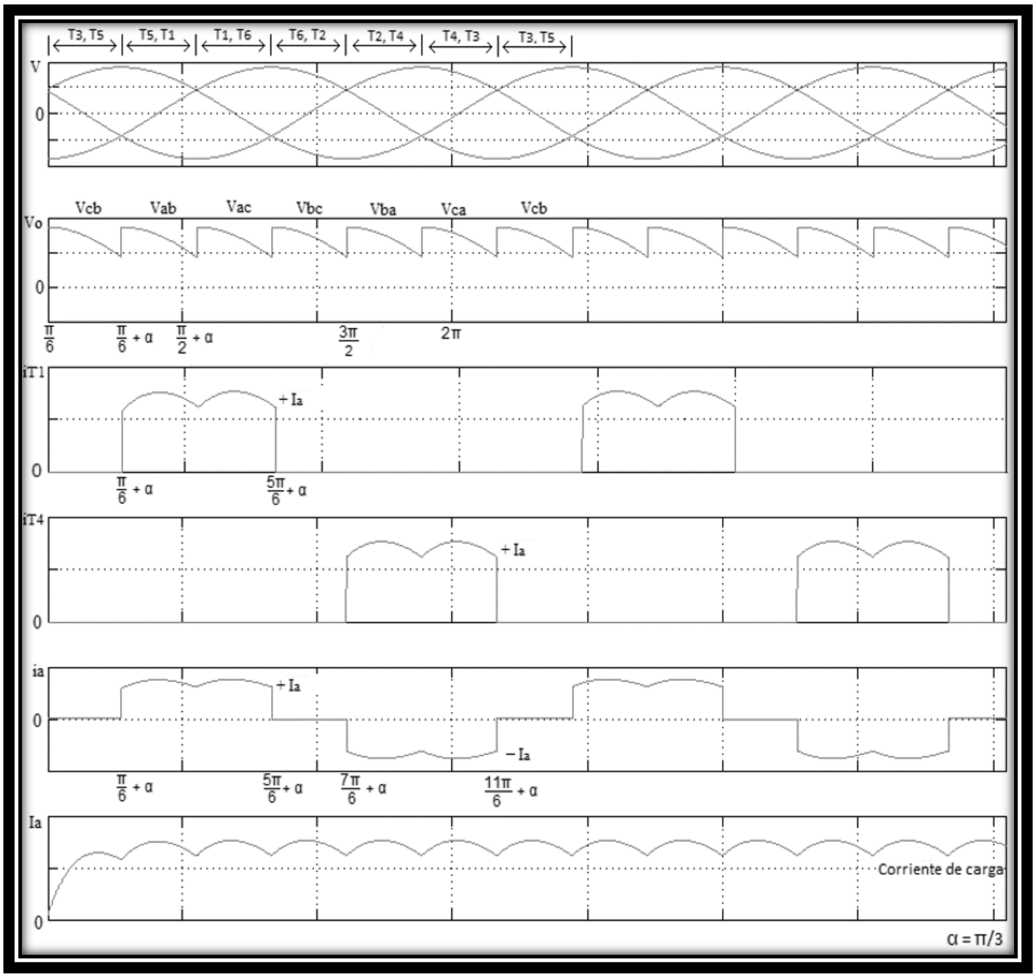

Fig. 10 Formas de onda de un rectificador trifásico totalmente controlado

9 MOTOR TAMAGNINI ROTOMOT 3L

El motor Tamagnini Rotomot 3L (**Fig. 11**) es un motor de imanes permanentes. Estos motores tienen la particularidad de contar con un sistema de “aletas concentradoras de flujo” que impiden las desmagnetizaciones accidentales. Por lo tanto, las altas corrientes de desmagnetización que el motor es capaz de soportar lo hacen especialmente conveniente para controles de velocidad regulados con SCR. El motor cuenta con el estándar de protección IP54, cableado en bloque y terminales con prensaestopas. Además, cuenta con la certificación CE.

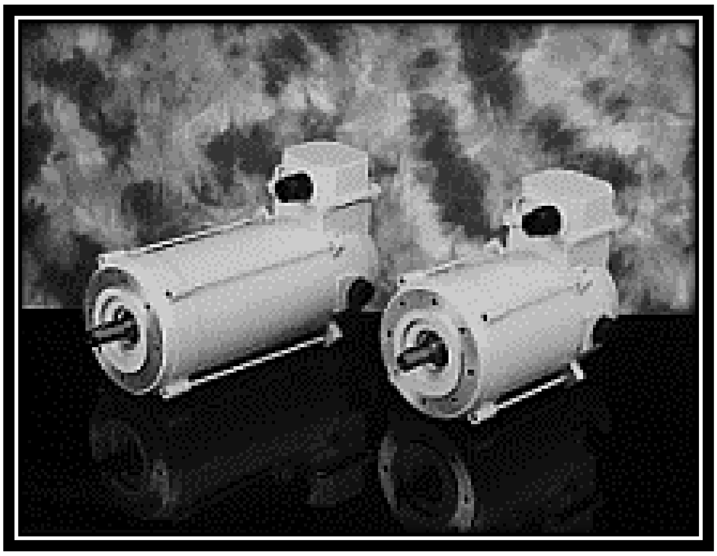

Fig. 11 *Motor Tamagnini Rotomot R3L*

Para la realización del control de velocidad es necesario conocer las características eléctricas y mecánicas del motor. En la siguiente tabla (**Tabla 2**) quedan recogidas las más importantes a la hora de implementar el sistema.

Tabla 2 *Características eléctricas y mecánicas del motor R3L, símbolos y valores.*

Dato del motor	Símbolo	Unidades	Valor
CARACTERÍSTICAS GENERALES			
Velocidad nominal	Nm	RPM	3000
Potencia nominal	Pu	W	600
Tensión nominal	Vn	V	170
Corriente nominal	In	A	4.5
CARACTERÍSTICAS MECÁNICAS			
Inercia del rotor	J	Kg/m^2	0.00169
Masa	m	Kg	10.3
CARACTERÍSTICAS ELÉCTRICAS			
Resistencia de armadura	Rm	Ohm	2.5
Inductancia de armadura	La	Mh	17.5

De estos datos puede obtenerse el módulo (**20**) y fase (**21**) de la impedancia interna del motor:

$$Z = \sqrt{R^2 + (\omega L)^2} = \sqrt{2.5^2 + (100\pi \cdot 17.5 \cdot 10^{-3})^2} = 6.04\,\Omega \qquad (\mathbf{20})$$

$$\theta = tan^{-1}\left(\frac{\omega L}{R}\right) = tan^{-1}\left(\frac{100\pi \cdot 17.5 \cdot 10^{-3}}{2.5}\right) = 72{,}829303\,° \qquad (\mathbf{21})$$

9.1 Dinamo tacométrica R3L

El motor cuenta con su propia dinamo tacométrica que permite obtener un nivel de tensión en función de las revoluciones del motor. La característica principal de este dispositivo es la constante de tensión, este valor es la relación entre la tensión generada y las revoluciones del motor (**Tabla 3**).

***Tabla 3** Valor de la constante de tensión de la tacodinámo del motor R3L*

Dato de la tacodinamo	Símbolo	Unidades	Valor
CARACTERÍSTICAS GENERALES			
Constante de tensión	En	V/KRPM	10

10 RECTIFICADOR TOTALMENTE CONTROLADO Y CONTROL DE VELOCIDAD DEL MOTOR

El puente rectificador ha sido diseñado para suministrar la potencia necesaria para el funcionamiento del motor Tamagnini Rotomot R3L. El diseño del rectificador se ha divido en dos partes independientes (**Fig. 12**):

1. Etapa de potencia
2. Etapa de control de fase
3. Control de velocidad del motor

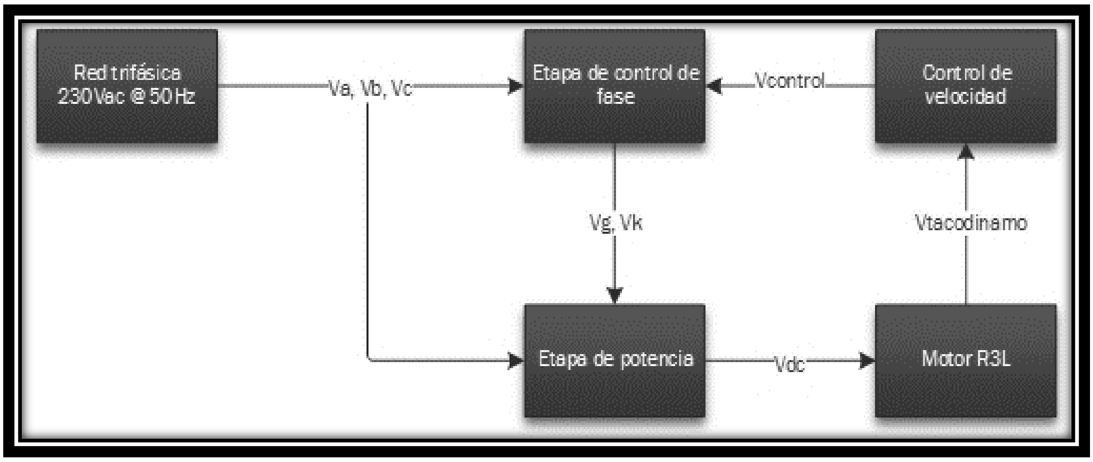

***Fig. 12** Flujograma del rectificador trifásico totalmente controlado con el control de velocidad*

10.1 Etapa de potencia

El diseño de la etapa de control se ha realizado en base a la red trifásica que se emplea como fuente de alimentación principal. La red trifásica equilibrada usada cuenta con una tensión eficaz simple de 230 V y una frecuencia de 50 Hz.

10.1.1 Transformadores de la etapa de potencia

Dada la tensión nominal del motor, y la tensión de la red trifásica de la que partimos puede obtenerse la relación de transformación adecuada para aplicar al motor (**22**).

$$m = \frac{Vn\,motor}{Vpico\ compuesta} = \frac{170}{230 \cdot \sqrt{2} \cdot \sqrt{3}} = \frac{170}{563.382} = 0.30175 \qquad (\mathbf{22})$$

Con esta relación de transformación, la tensión eficaz de simple (**23**) será la siguiente:

$$V_o = V_i \cdot m = 230 \cdot 0.301749 = 69.4\,V \qquad (\mathbf{23})$$

La configuración para los transformadores de potencia es estrella-estrella, es decir con un punto común a las tres fases (**Fig. 13**).

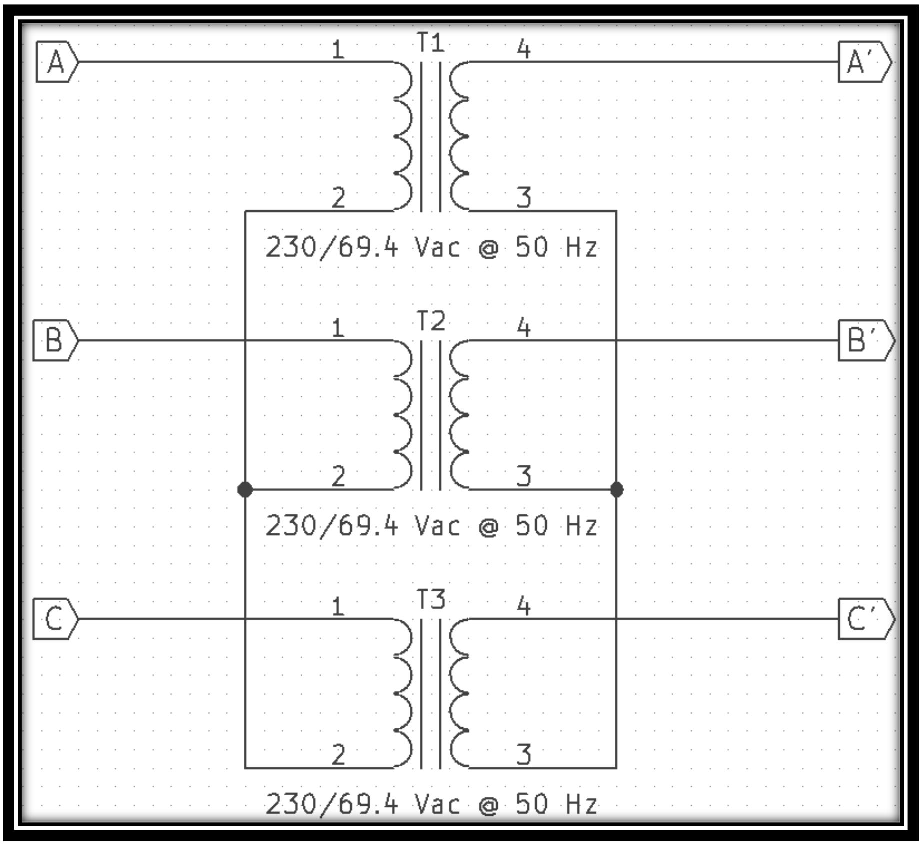

Fig. 13 *Configuración estrella-estrella de los transformadores de potencia*

10.1.2 Puente rectificador controlado

Sabiendo la tensión nominal del motor y la tensión que aplicaremos al puente se comprueba si el ángulo de disparo es admisible para la tensión máxima (**24**).

$$\alpha_{\min} = cos^{-1}\left(\frac{V_{CC}}{V_{AC}}\right) = cos^{-1}\left(\frac{170}{170}\right) = 0\ ° \tag{24}$$

La tensión promedio máxima (**25**) y la tensión eficaz máxima (**26**)) que se aplicará al motor será con ángulo de disparo $\alpha = 0°$.

$$V_{CC} = \frac{\sqrt{3} \cdot V_m \cdot \cos(\alpha)}{\pi} = \frac{3\sqrt{3} \cdot \sqrt{2} \cdot (230 \cdot 0.301749) \cdot \cos(0)}{\pi} \tag{25}$$

$$\boxed{V_{CC} = 162.338}$$

$$\begin{aligned} V_{RMS} &= \sqrt{3}V_m\sqrt{\frac{1}{2} + \frac{3\sqrt{3}}{4\pi}\cos(2\alpha)} \\ &= \sqrt{3} \cdot \sqrt{2} \cdot (230 \cdot 0.301749)\sqrt{\frac{1}{2} + \frac{3\sqrt{3}}{4\pi}\cos(2 \cdot 0)} \end{aligned} \tag{26}$$

$$\boxed{V_{RMS} = 162.481\ V}$$

Dado que se trata del ángulo de disparo mínimo que implica una tensión máxima, la tensión promedio y la tensión eficaz son prácticamente iguales. Lo mismo ocurre con la corriente promedio (**27**) máxima ($\alpha = 0°$) y la corriente eficaz máxima de salida (**28**). Éstas vienen dadas por la impedancia del motor.

$$I_{CC} = \frac{V_{DC}}{R} = \frac{162.338217}{6.04} = 26.877\ A \tag{27}$$

$$I_{RMS} = \frac{V_{RMS}}{R} = \frac{162.481}{6.04} = 26.9\ A \tag{28}$$

Del mismo modo la corriente media (**29**) y eficaz (**30**) máxima que circulará por los tiristores serán de mismo valor.

$$I_{CC_{tiristor}} = \frac{I_{CC}}{3} = \frac{26.8777}{3} = 8.97\ A \tag{29}$$

$$I_{RMS\_tiristor} = \frac{I_{RMS}}{3} = \frac{26.9}{3} = 8.966\ A \tag{30}$$

Para la elección de los tiristores se ha tenido en cuenta la frecuencia de funcionamiento, la tensión inversa máxima (Vdrm) y la corriente máxima de conducción del tiristor (Imax). La frecuencia de funcionamiento es 50Hz por lo tanto está muy por debajo de la frecuencia de funcionamiento de estos dispositivos. El tiristor elegido es el BT151 (**Tabla 4**) ya que tanto la tensión inversa como la corriente máxima que puede soportar están por encima de las máximas que va a suministrar el circuito.

***Tabla 4** Referencia y características del tiristor escogido para el puente rectificador*

Nombre	Imax(A)	Umax(V)	Igt(mA)	Encapsulado
BT 151-500R	12	500	15	T0-220

La corriente de activación de puerta máxima (Igt) es de 15 mA por lo tanto es necesario poner una resistencia (**31**) entre la puerta y el cátodo para limitarla y evitar la destrucción del componente.

$$R_{min} = \frac{Vgt}{Igt} = \frac{12}{15\cdot 10^{-3}} = 800\ \Omega \qquad (\mathbf{31})$$

Como resistencias normalizadas de este valor no existen se ha seleccionado la inmediatamente superior de valor $R = 820\ \Omega$.

La configuración del puente rectificador está recogida en la tabla (**Tabla 5**). y figura (Fig. 14).

***Tabla 5** Componentes del puente rectificador*

COMPONENTES DEL PUENTE RECTIFICADOR CONTROLADO	
Nombre	**Cantidad**
BT151-500R	6
Resistencia 820 Ω	6

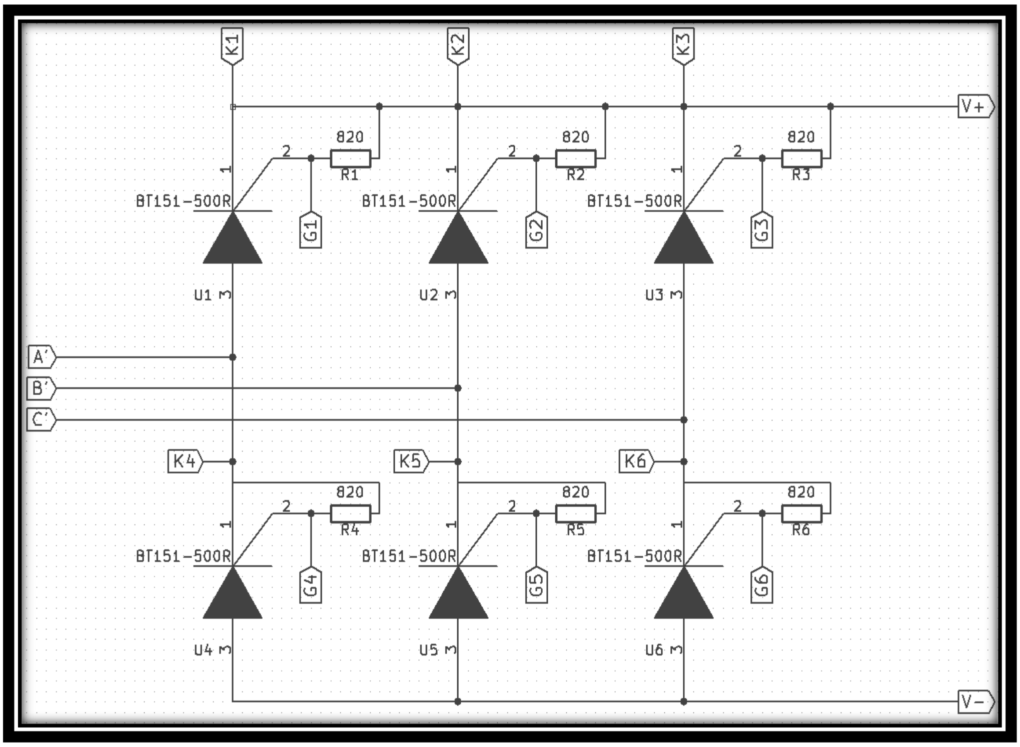

Fig. 14 Esquemático del puente rectificador

10.2 Etapa de control de fase

10.2.1 Transformadores de la etapa de control

El uso de transformadores para la etapa de control viene condicionado por la necesidad de reducir la tensión hasta valores adecuados para el funcionamiento de los elementos de la etapa de control como la de aislar eléctricamente la etapa de control de la etapa de potencia.

10.2.1.1 Transformadores para alimentación

La tensión en el primario para estos transformadores es de 230 Vac RMS. Se ha seleccionado un rango de tensiones adecuado para el devanado secundario de los transformadores de alimentación de la etapa de control. Dado el posterior uso de dicha tensión, a la cual se le realizará un rectificado, filtrado y estabilizado, se ha seleccionado un rango de tensiones eficaces aceptados en un intervalo $V_s = [13.014, 17.677]\ V$. esto implica un intervalo de valores de tensión máximos en el secundario de $V_s = [18.5, 25]\ V$. La elección de este rango de valores viene condicionada por los valores máximo y mínimo de funcionamiento de los reguladores de tensión que serán usados en el posterior diseño.

La potencia de los transformadores se ha seleccionado realizando una estimación de la carga que tendrá que soportar cada una de las fases. Esta estimación se ha realizado sumando las potencias máximas que pueden consumir todos los componentes implicados. La fase A tendrá más carga ya que también alimentará el circuito del control de PI del motor. En las ecuaciones (**32**), (**33**) y (**34**) se encuentran los sumatorios de potencias por fase.

$$P_{TfaseA} = P_{TCA785} + P_{555} + P_{PI} + P_{Perdidas} = 6 + 3 + 0.71 + 1.5 = 11.21\ VA \qquad (\mathbf{32})$$

$$P_{TfaseB} = P_{TCA785} + P_{555} + P_{Perdidas} = 6 + 3 + 1 = 10\ VA \qquad (\mathbf{33})$$

$$P_{TfaseC} = P_{TCA785} + P_{555} + P_{Perdidas} = 6 + 3 + 1 = 10\ VA \qquad (\mathbf{34})$$

Para evitar posibles sobrecargas se ha sobredimensionado la potencia de cada transformador eligiendo el FS28-1300-C2 de TRIAD MAGNETICS (

Tabla 6). Este transformador cuenta con dos devanados primarios y dos secundarios.

Nombre	Nº prim.	Nº secun.	Potencia	Vprimario	Vsecundario
FS28-1300-C2	2	2	36 VA	230/115 V	14 V

Nombre	Nº prim.	Nº secun.	Potencia	Vprimario	Vsecundario
FS28-1300-C2	2	2	36 VA	230/115 V	14 V

***Tabla 6** Características de los transformadores FS28-1300-C2*

Como se dispone de dos primarios y dos secundarios se ha recurrido al uso de 2 transformadores de este tipo.

En la (**Tabla 7**) y en la (**Fig. 15**) están los componentes la configuración de estos transformadores:

Tabla 7 Número de transformadores FS28-1300-C2 usados

COMPONENTES	
Nombre	**Cantidad**
FS28-1300-C2	2

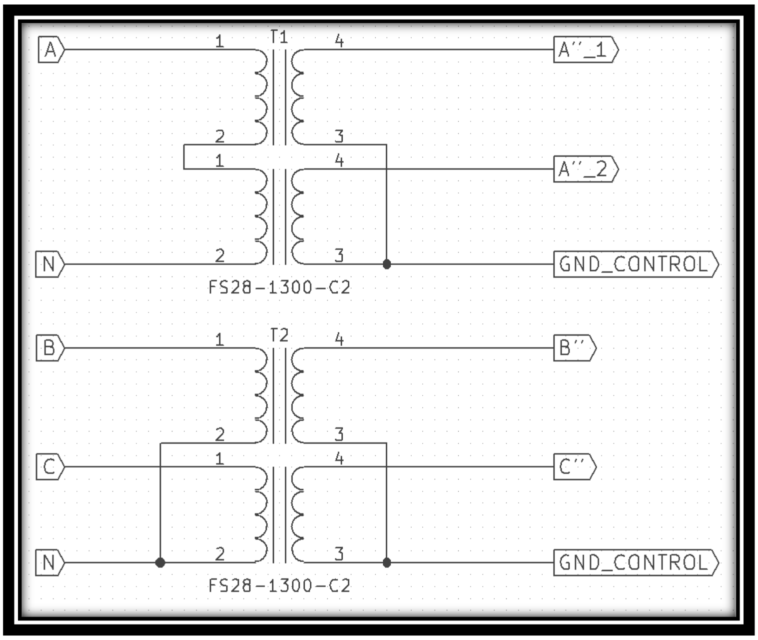

Fig. 15 Configuración de los transformadores de alimentación

10.2.1.2 Transformadores de impulsos

Para el aislamiento y transmisión de las señales de disparo desde la etapa de control a la etapa de potencia se ha hecho uso de transformadores de impulso. La característica principal de estos

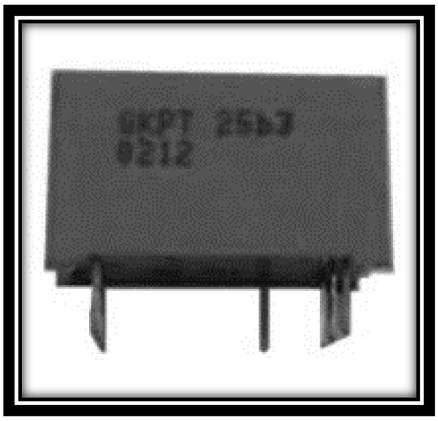

Fig. 16 Transformador de impulsos SKPT 25b3

transformadores es que su relación de transformación es 1, es decir, la tensión que en el devanado primario es la misma que la tensión en el devanado secundario.

Los transformadores seleccionados son los SEMIKRON SKPT 25b3 (**Fig. 16**). Estos transformadores cuentan con dos devanados secundarios y uno primario.

Las características de este transformador se reúnen en la (**Tabla 8**):

Tabla 8 *Características de los transformadores de impulsos SKPT 25b3*

Nombre	Np/Ns	Rp	Rs	tr	Vww	Visol
SKPT 25b3	1:1:1	0.55 Ω	0.55 Ω	1.5 us	500 V	4000 V

La configuración y los componentes están en la (**Tabla 9**) y en la (**Fig. 17**).

Tabla 9 *Número de transformadores SKTP 25b3*

COMPONENTES	
Nombre	**Cantidad**
SKPT 25b3	6

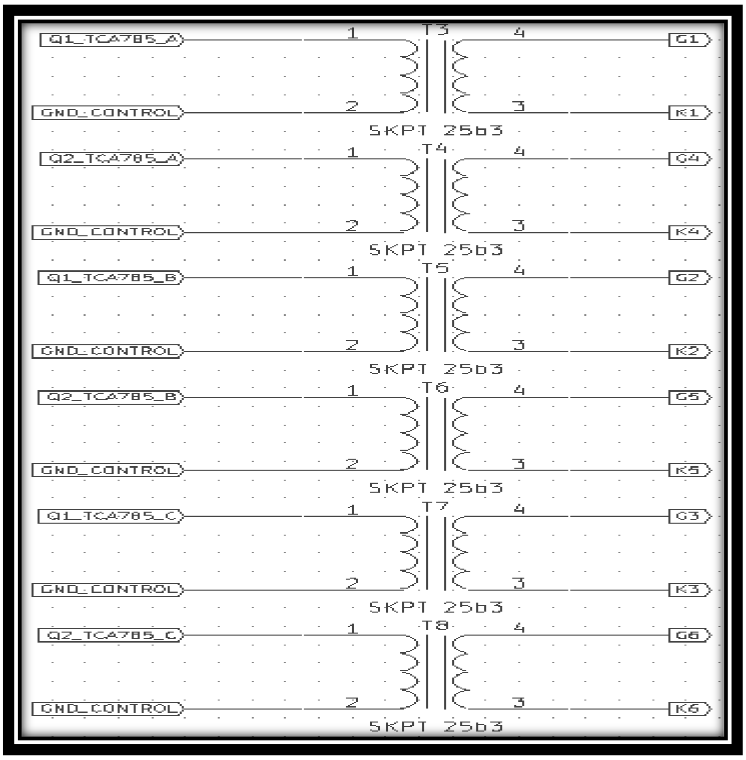

Fig. 17 *Configuración de los transformadores de impulsos*

10.2.1.2.1 Alternativas al transformador de impulsos

Como alternativa para la realización de esta etapa de aislamiento y transmisión de las señales de disparo de los tiristores puede hacerse uso de optoacopladores u opotoaisladores. Estos dispositivos polarizan la base de un transistor o triac (**Fig. 18**) por medio de un fotodiodo para transmitir la señal.

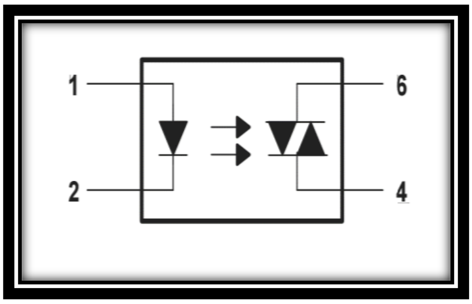

Fig. 18 *Modelo de un optotriac*

Haciendo uso de 6 dispositivos de este tipo, podría aislarse la etapa de control de la etapa de potencia como muetra la (**Fig. 19**). Transmitiendo las 6 señales de disparo a los tiristores.

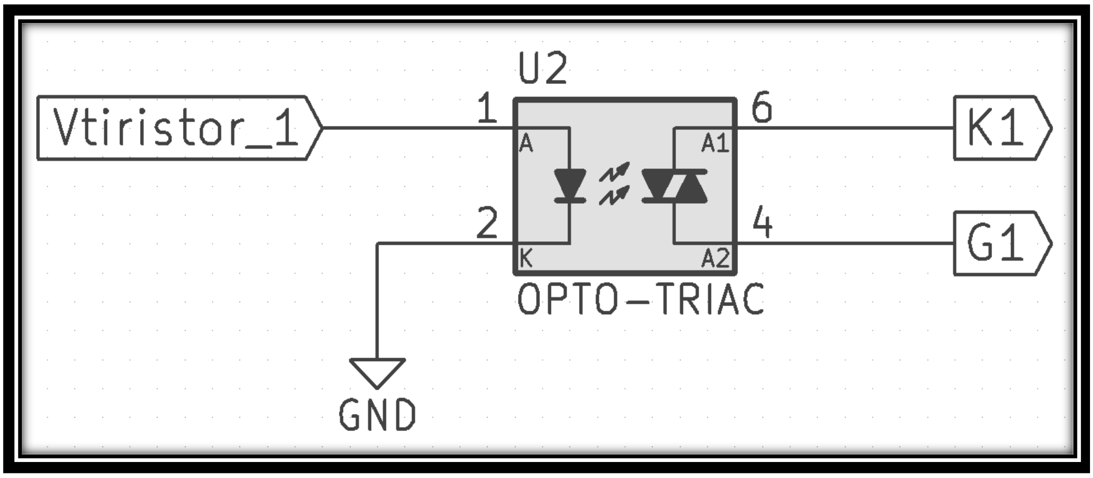

Fig. 19 *Aislamiento realizado con un optotriac*

10.2.2 Circuito de alimentación para la etapa de control

Para administrar la potencia necesaria para hacer funcionar adecuadamente los circuitos pertenecientes a esta etapa, además del circuito del regulador PI, se ha hecho uso de un rectificador monofásico de media onda, un filtro y un regulador.

La tensión rectificada (**35**) por el diodo es filtrada por el condensador que elimina el rizado de la tensión.

$$V_{rect} = \sqrt{2} \cdot V_{transformador} = \sqrt{2} \cdot 14 = 19.8\,V \tag{35}$$

Esta tensión presente en las entradas de los reguladores 7815 y 7915 hace que se tenga una salida estabilizada de +15V (7815) y -15V (7915). Entre la patilla de salida y GND se conecta un condensador de 330 nF de desacoplo por el cual se derivan pequeños ruidos no deseados en la señal de salida.

La (**Tabla 10**) y la (**Fig. 20**) muestran la configuración y los componentes de este circuito:

Tabla 10 *Componentes del circuito de alimentación para la etapa de control*

COMPONENTES	
Nombre	**Cantidad**
1N4007	5
C2700uF25V	5
7815	4
7915	1
C300nF	5

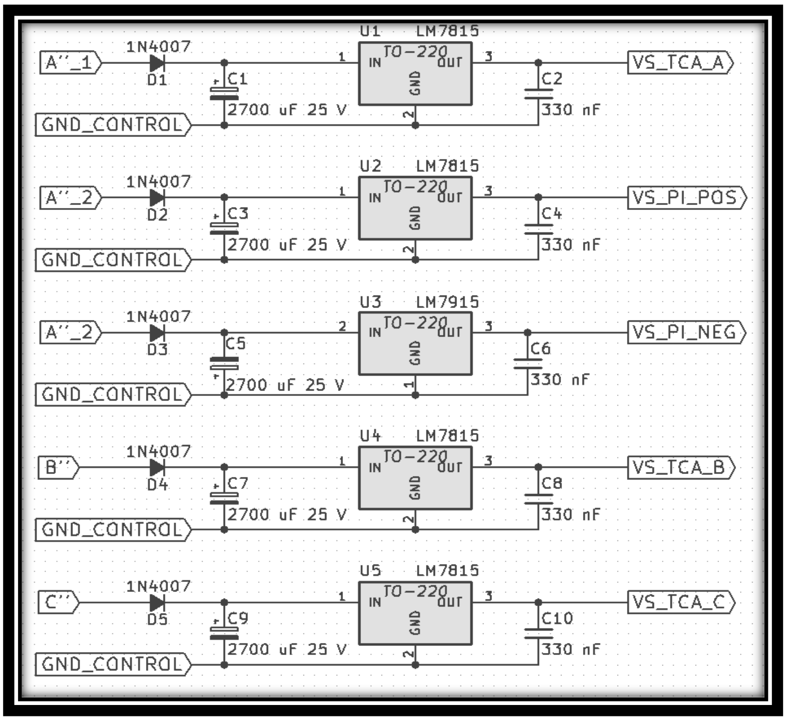

Fig. 20 *Esquemático del circuito de alimentación para la etapa de control*

10.2.3 Circuito de sincronismo y disparo

Para poder disparar los tiristores en la secuencia correcta es necesario la obtención de pulsos sincronizados con las tensiones compuestas o con un ángulo de retraso de 30° respecto de las tensiones simples. Estos disparos irán desde un ángulo mínimo de 0° hasta un ángulo máximo de 120°.

Para conseguirlo se ha hecho uso del circuito integrado TCA785. Con tres, uno por fase, se obtienen las seis señales de disparo necesarias para disparar los seis tiristores.

La configuración de los TCA785 y sus componentes están recogidos en la tabla (**Tabla 11**) y figura (**Fig. 21**) siguientes:

Tabla 11 Componentes del circuito de sincronismo y disparo

COMPONENTES	
Nombre	**Cantidad**
TCA785	3
1N4148	12
R33k	3
R100	6
R47k	3
R55k	3
C47nF	3
C150nF	6

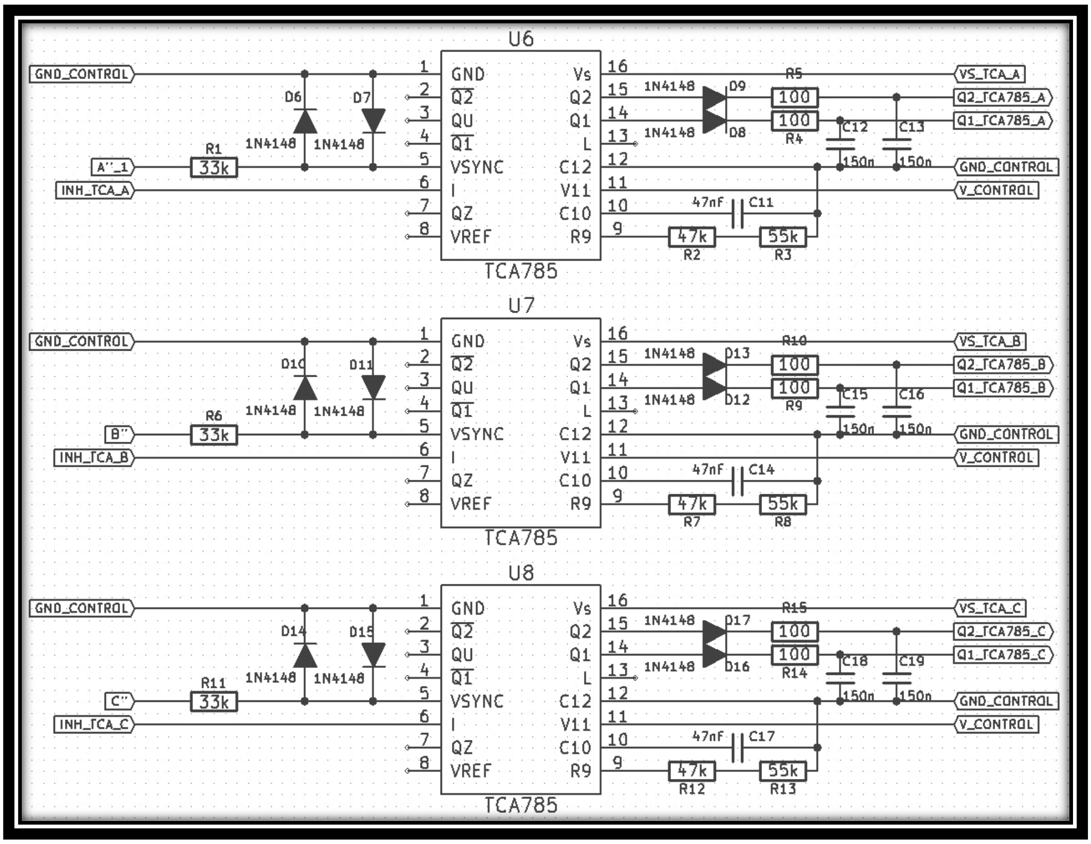

Fig. 21 Esquemático del circuito de sincronismo y disparo de los tiristores

10.2.3.1 Entrada de inhibición (patilla 6)

Para el correcto funcionamiento de los tiristores se han troceado las salidas Q1 y Q2 de los TCA785. Para conseguir esto, se ha hecho uso de la patilla 6 (entrada de inhibición) del tca785. Esta patilla permite activar y desactivar las salidas Q1 y Q2. Con un CI 555 en modo astable conectado a esta entrada se ha conseguido dicho resultado.

Dada la ecuación (**37**), se ha seleccionado una frecuencia (**36**) para el multivibrador astable, a partir de la cual se han calculado los valores de los otros componentes.

$$f = 2\ kHz;\ T = \frac{1}{f} = \frac{1}{2000}\, s \qquad (\mathbf{36})$$

$$T = 0.693(R_1 + 2R_2)C_1\ s \qquad (\mathbf{37})$$

Para la resolución de esta ecuación se han seleccionado valores normalizados de resistencia para R1 y R2 y se ha obtenido el valor de C1 (**38**).

$$R_1 = 3.9\ k\Omega;\ R_2 = 3\ k\Omega \qquad (\mathbf{38})$$

Por lo tanto, despejando C1 y sustituyendo los valores conocidos puede obtenerse el valor de la capacidad (**39**).

$$C_1 = \frac{T}{0.693(R_1+2R_2)} = \frac{\frac{1}{2000}}{0.693(3900+2\cdot 3000)} = 7.23\cdot 10^{-8} = 72.3\ nF \qquad (\mathbf{39})$$

Como el valor del condensador no está normalizado se ha seleccionado el más próximo que es $C_1 = 68nF$. En la ecuación (**40**) se recalcula la frecuencia de la señal PWM generada por los CI 555.

$$f = \frac{1}{T} = \frac{1}{0.693(3900+2\cdot 3000)\cdot 68\cdot 10^{-9}} = 2143.5\ Hz \qquad (\mathbf{40})$$

En la tabla (Tabla 12) y la figura (Fig. 22) están los componentes y configuración de los 555.

Tabla 12 *Componentes de los 555 en modo astable*

COMPONENTES	
Nombre	**Cantidad**
CI 555	3
R3.9k	3
R3k	3
C68Nf	3

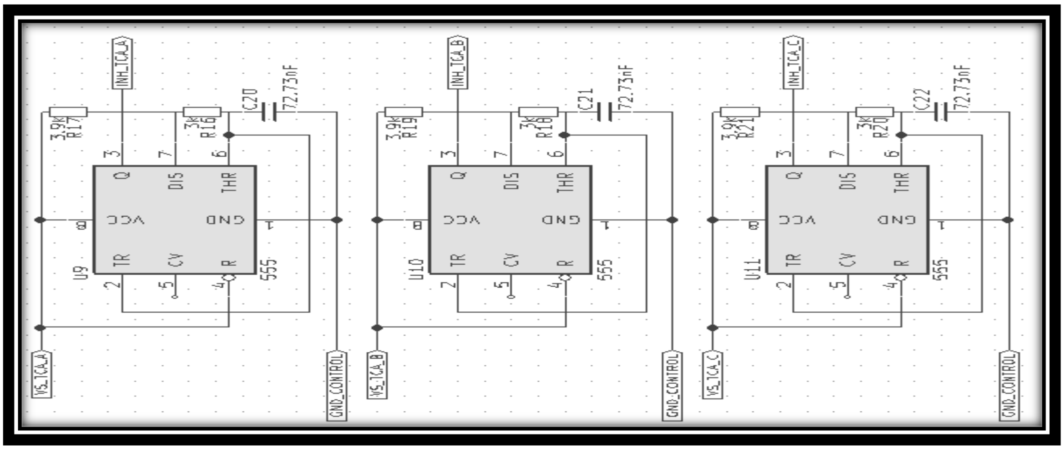

Fig. 22 *Esquemático de los 555 en modo astable*

10.2.3.2 Alternativas al circuito de sincronismo y disparo

Una alternativa al control de fase usando TCA785, es el uso de optoacopladores con detector de pasos por cero como muestra la figura (**Fig. 23**). De este modo, se polarizará la base del transistor y se comparará con la tensión de control en el comparador obteniendo a la salida la tensión para llevarla a la etapa de los transformadores de aislamiento u optoacopladores.

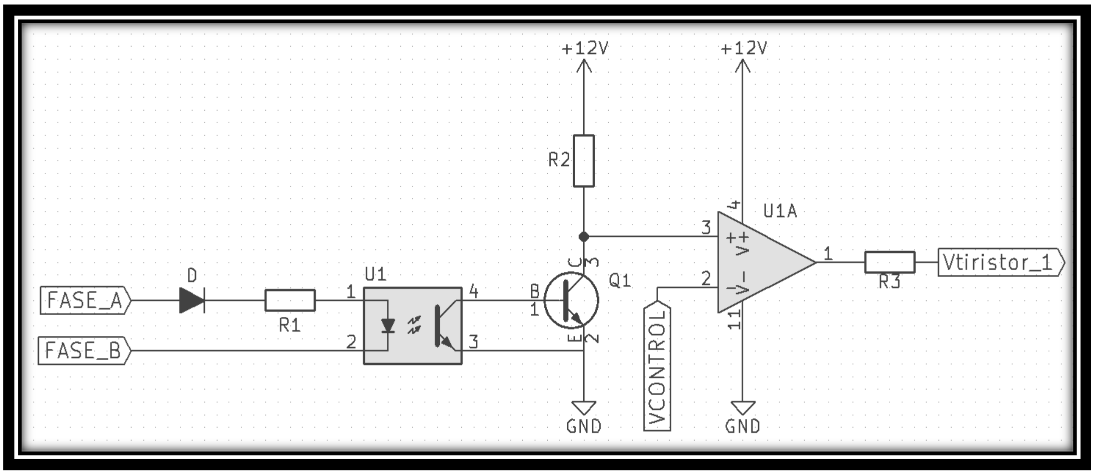

Fig. 23 Circuito de sincronismo alternativo al TCA785

Debería replicarse el circuito hasta tener 6 de este tipo. Haciendo uso de las diferentes combinaciones de fases: AB, BC, CA, BA, CB, AC. Así se obtendrían los 6 pulsos necesarios.

10.3 Control PI de velocidad del motor

El algoritmo de control a usar es el PI en paralelo (**41**). El valor de salida del controlador proporcional varía en razón proporcional al tiempo en que ha permanecido el error y la magnitud del mismo, su función de transferencia es:

$$\frac{Y(s)}{E(s)} = K_P\left(\frac{1}{T_i \cdot s} + 1\right) \qquad (\mathbf{41})$$

Donde KP es la ganancia proporcional y Ti se denomina tiempo de acción integral. Ambos valores son ajustables. El tiempo integral regula la velocidad de acción de control.

El primer paso a la hora de realizar el control de velocidad ha sido conseguir un modelo del motor con el que poder trabajar. Haciendo uso de la herramienta Simulink de MATLAB se ha podido simular el comportamiento del motor en lazo abierto.

En la figura (**Fig. 24**) está el modelo de motor a usar en las simulaciones.

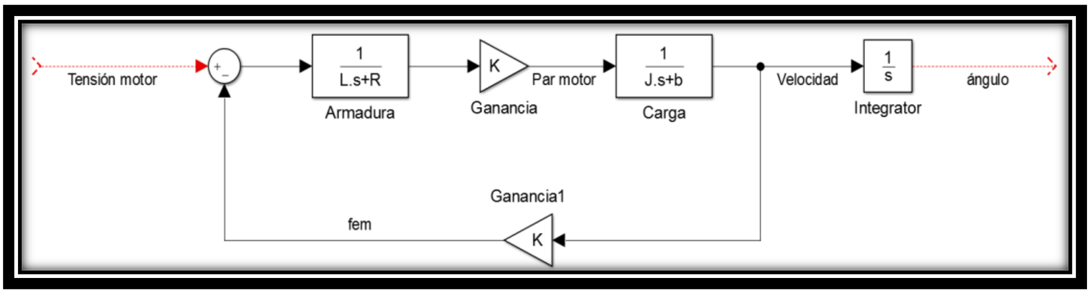

Fig. 24 *Diagrama de bloques del modelo del motor R3L*

Para la obtención del valor de Ke se ha empleado la ecuación (**42**) derivada del modelado físico de un motor DC:

$$K_e = \frac{V_a - R_a i}{\omega} = \frac{170-(2.5\cdot 4.5)}{\frac{3000\cdot 2\pi}{60}} = 0.50532\,\frac{Vs}{rad} \tag{42}$$

Como es un motor DC de imanes permanentes el valor $K_e = K_t$ pero con diferentes unidades como muestra la ecuación (**43**).

$$K_t = 0.50532\,\frac{\mathrm{Nm}}{\mathrm{A}} \tag{43}$$

La obtención del coeficiente de fricción viscoso se ha realizado mediante la ecuación (**44**).

$$B = \frac{K_e i}{\omega} = \frac{0.50532\cdot 4.5}{\frac{3000\cdot 2\pi}{60}} = 0.00724\,\frac{Nms}{rad} \tag{44}$$

Los valores a utilizar para las diferentes simulaciones del motor R3L son los de la tabla (**Tabla 13**).

Tabla 13 *Datos para el modelo de simulación del motor R3L*

DATOS PARA EL MODELO DE MOTOR			
Nombre	**Símbolo**	**Valor**	**Unidades**
Inductancia armadura	L	17.5	H
Resistencia armadura	R	2.5	Ohm
Constante eléctrica	Ke	0.505	V/(rad/s)
Constante mecánica	Kt	0.505	Nm/A
Coeficiente de inercia	J	0.00169	Kg/m^2
Coeficiente de fricción viscosa	b	0.00724	Nms/rad

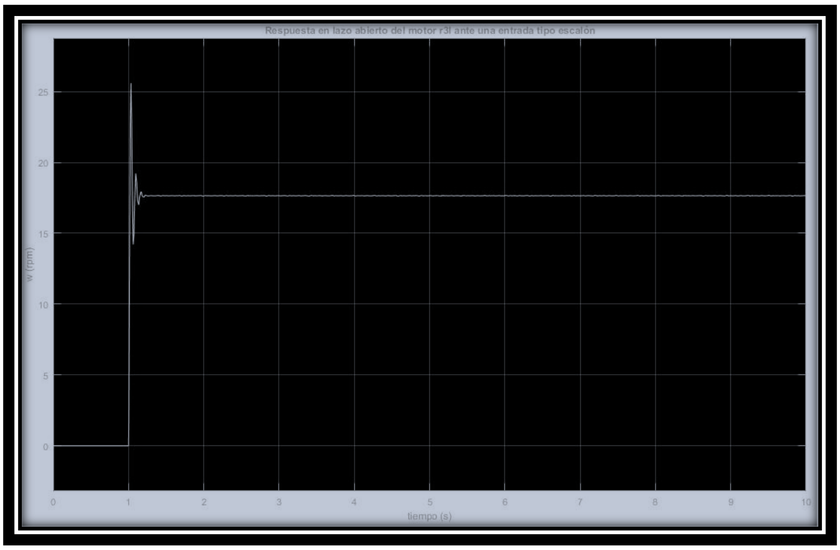

Fig. 27 Respuesta en lazo abierto del motor R3L

Para la simulación en lazo abierto ante una entrada tipo escalón se ha usado el diagrama de bloques (**Fig. 25**).

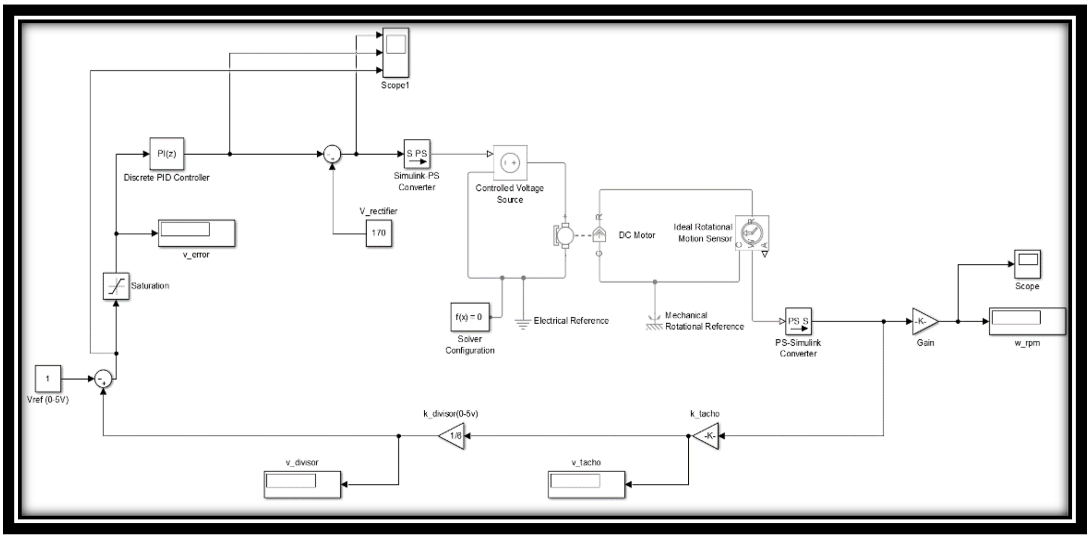

Fig. 25 Diagrama de Simulink para la simulación del motor R3L en lazo cerrado con el regulador

El sistema sobreoscila en lazo abierto (**Fig. 26**), por lo que es necesario la introducción de un regulador para eliminar dicha sobreoscilación.

Para la obtención de la Kp y Ki del regulador se ha empleado una simulación haciendo uso del sistema de la figura (**Fig. 27**).

Con la herramienta PID Tuner se han seleccionado unos valores de la parte proporcional e integral del regulador para que cumplan las condiciones de la ecuación (**45**).

$$\begin{gathered} t_s \leq 1\,s \\ t_e \leq 2\,s \end{gathered} \tag{45}$$

La ecuación (**46**) muestra los valores obtenidos por el PID Tuner de Simulink.

$$\begin{gathered} Kp = 1 \\ Ki = 100 \end{gathered} \tag{46}$$

Para la simulación del PI realizado con componentes electrónicos se ha usado el diagrama de simulink de la figura (**Fig. 28**).

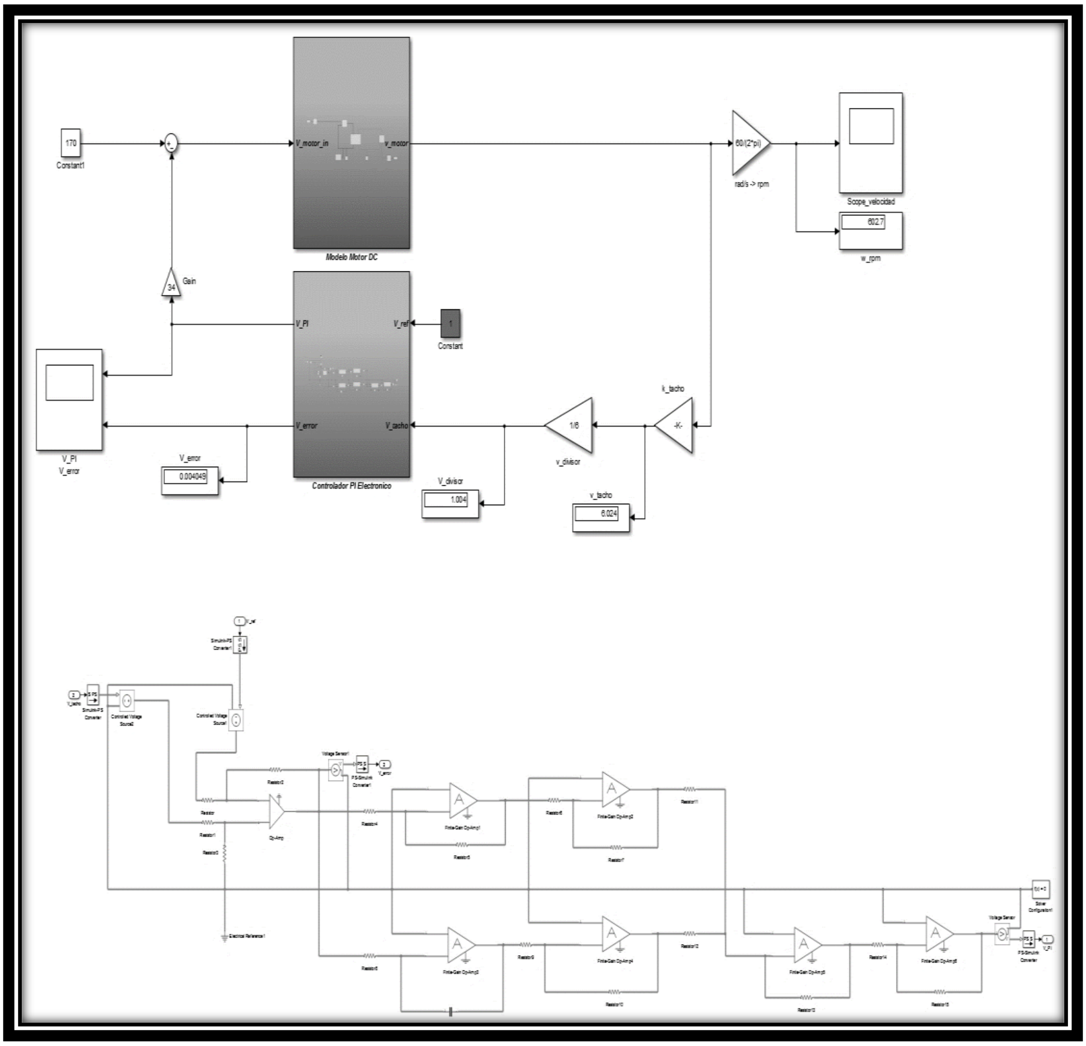

__Fig. 28__ Diagrama de simulink empleado para la simulación en lazo cerrado con el PI electrónico (Kp=1; Ki=100)

10.3.1 Regulador PI electrónico

La implementación física del regulador PI es totalmente analógica. La etapa de regulación ha sido implementada con amplificadores operacionales trabajando en diferentes configuraciones.

Para realizar el control PI electrónico se ha usado la tensión de la tacodinamo del motor y una tensión de referencia. La tacodinamo tiene un rango de valores tensión entre 0V (0 rpm) y 30V (3000 rpm) ya que su constante de tensión es 10 mV /rpm.

El rango de tensiones de la referencia va de 0V a 15V mediante un potenciómetro de 10kΩ por lo que se ha adecuado el nivel de tensiones de la dinamo tacométrica mediante un divisor de tensiones de ganancia ½ y valores de resistencia 10kΩ. Los componentes y la configuración de estos divisores están en la tabla (**Tabla 14**) y la figura (**Fig. 29**).

***Tabla 14** Componentes de los divisores resistivos de las tensiones de referencia y tacodinamo*

COMPONENTES	
Nombre	**Cantidad**
Resistor 10kΩ	2
Potenciómetro 10kΩ	1

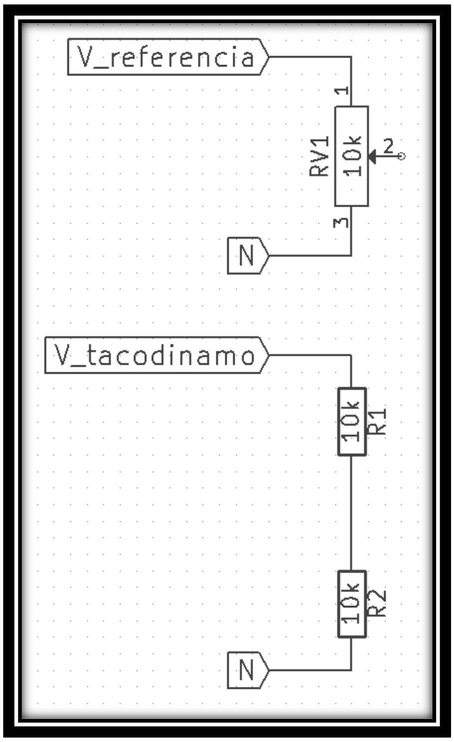

***Fig. 29** Esquemático de los divisores resistivos de las tensiónes de referencia y tacodinamo*

10.3.1.1 Amplificador diferencial inversor

Para restar la tensión de referencia a la tensión de la tacodinamo se ha hecho uso de un amplificador en configuración diferencial y de ganancia unitaria (**47**). Los valores de resistencias de esta etapa son todos de 10kΩ.

$$\begin{gathered} G = 1 \\ Vo = G \cdot (V^{+} - V^{-}) = V^{+} - V^{-} \end{gathered} \quad (\mathbf{47})$$

Los componentes y la configuración del amplificador diferencial están en la tabla (**Tabla 15**) y la figura (**Fig. 30**).

Tabla 15 *Componentes del amplificador operacional diferencial*

COMPONENTES	
Nombre	**Cantidad**
Resistor 10kΩ	4
TL081	1

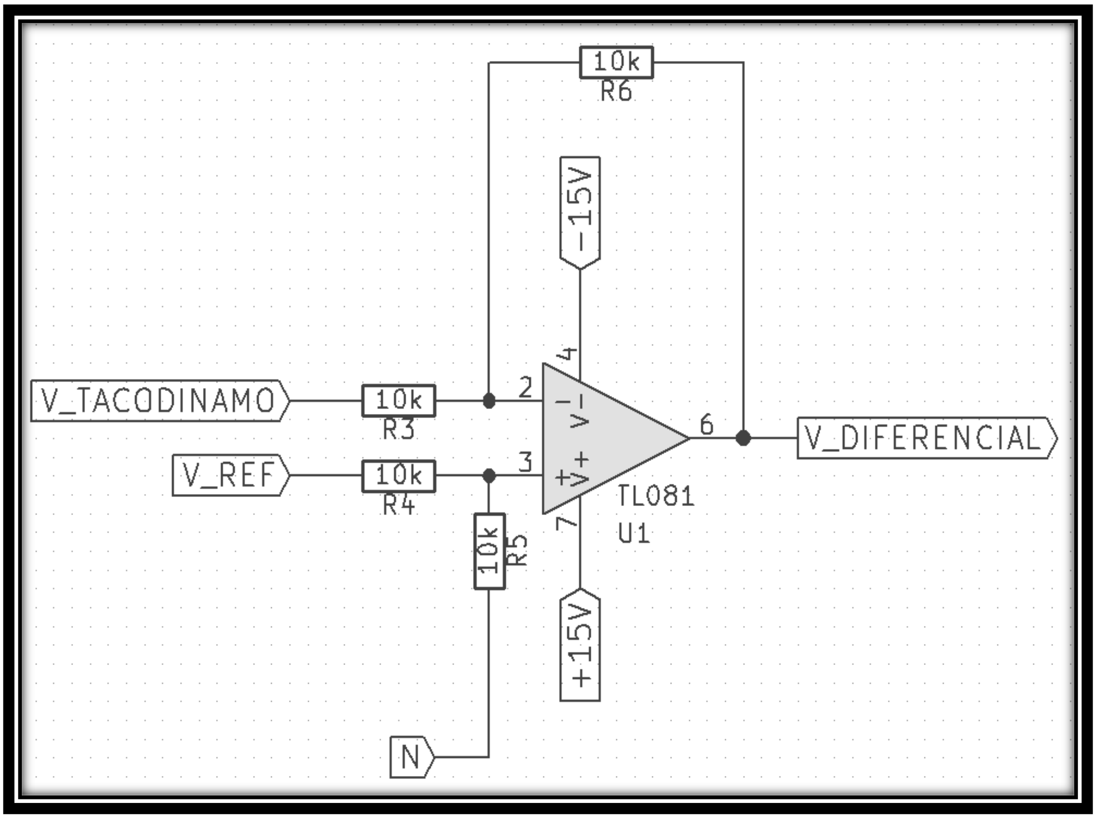

Fig. 30 *Esquemático del amplificador operacional diferencial*

10.3.1.2 Ganancia proporcional

La ganancia proporcional se ha obtenido mediante un amplificador inversor cuya ganancia es la ganancia proporcional del regulador PI. La ganancia de esta etapa es negativa, pero de mismo valor que la ganancia proporcional del regulador PI (**48**). La polaridad se invertirá en una etapa posterior del regulador. Los valores seleccionados para esta etapa son 10kΩ.

$$\begin{gathered} Vo = Vi \cdot G = -Vi \cdot \frac{R_2}{R_1} \\ G = K_p = 1 \\ Vo = -Vi \end{gathered} \qquad (\mathbf{48})$$

Los componentes y la configuración del amplificador inversor están en la tabla (**Tabla 16**) y la figura (**Fig. 31**).

Tabla 16 *Componentes del amplificador operacional inversor Kp*

COMPONENTES	
Nombre	**Cantidad**
Resistor 10kΩ	2
TL081	1

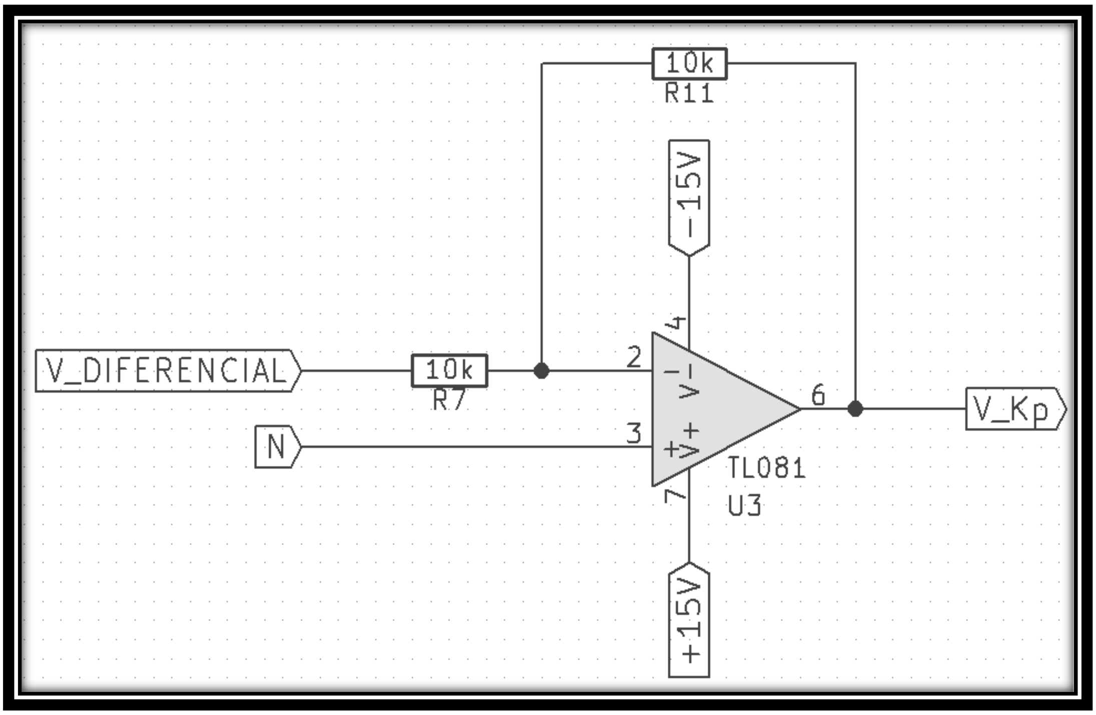

Fig. 31 *Esquemático del amplificador operacional inversor Kp*

10.3.1.3 Integrador

La ganancia integral se aplica mediante un amplificador configurado en modo integrador. Sabiendo la ganancia integral se han obtenido los valores de resistencia y capacitor necesarios para su diseño y montaje. Como el análisis que se realiza es de corriente continua la ganancia se simplifica a la ecuación (**49**).

$$G = Ki = \frac{1}{RC} = 100 \tag{49}$$

Se selecciona como valor de condensador 1 uF y se despeja el valor de resistencia en la ecuación (**50**).

$$R = \frac{1}{1 \cdot 10^{-6} \cdot 100} = 10\ k\Omega \tag{50}$$

Los componentes y la configuración del integrador están en la tabla (**Tabla 17**) y la figura (**Fig. 32**).

***Tabla 17** Componentes del amplificador operacional integrador Ki*

COMPONENTES	
Nombre	**Cantidad**
Resistor 10kΩ	1
TL081	1
Capacitor 10uF	1

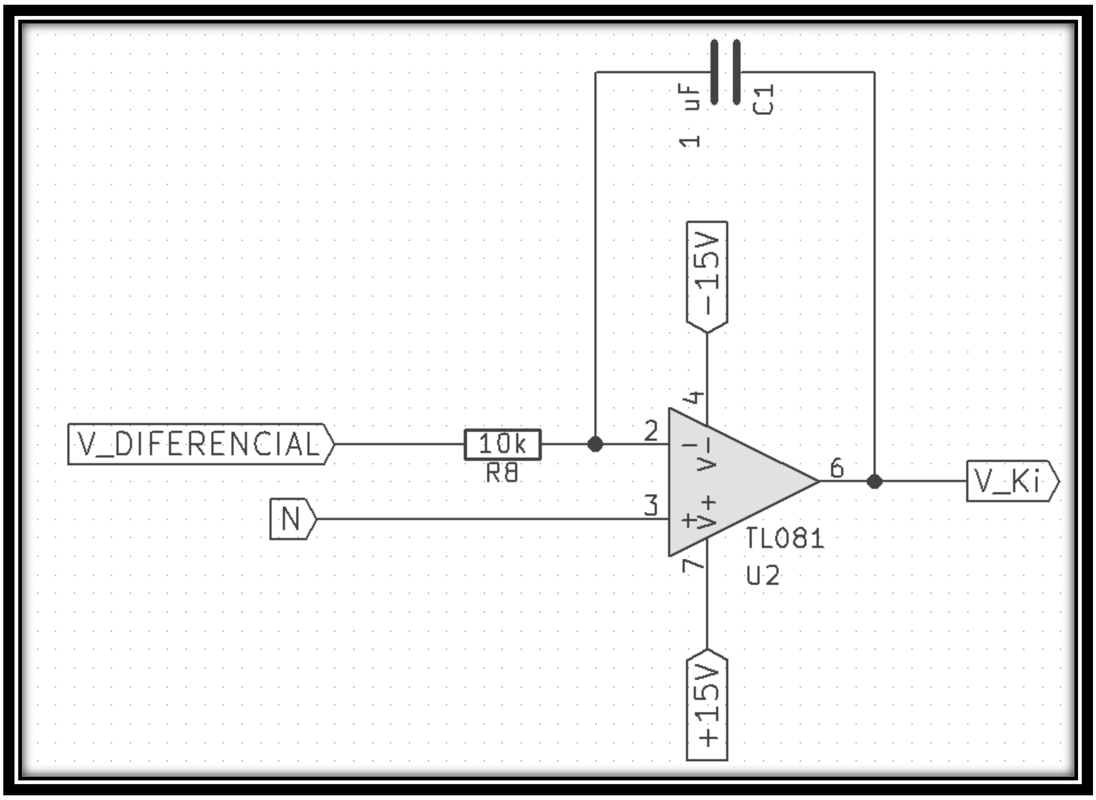

***Fig. 32** Esquemático del amplificador integrador Ki*

10.3.1.4 Sumador inversor y buffer

Para sumar ambas ganancias se ha hecho uso de un amplificador sumador inversor. Con esto se consigue, además de sumar las tensiones de etapas anteriores, invertir la polaridad. Las resistencias de esta configuración son todas de igual valor, 10 kΩ. Por lo tanto, la función de transferencia es la ecuación (**51**).

$$Vo = G \cdot Vi = (V_1 + V_2) \cdot G = -(V_1 + V_2) \quad \textbf{(51)}$$

Para evitar problemas de desacoplo de impedancias de se ha colocado a la salida de este sumador un buffer de ganancia unitaria. Su función de transferencia es la ecuación (**52**).

$$V_o = G \cdot V_i = V_i \quad \textbf{(52)}$$

Este amplificador cuenta con la tecnología *rail-to-rail* esto implica, a nivel práctico, que pueda alimentarse desde 0V a +15V pudiendo llegar ambos voltajes de saturación sin pérdidas.

A la salida de dicho buffer se ha colocado un divisor de tensión cuyas resistencias son de idéntico valor para tener una ganancia de 0.5, cuya función de transferencia es la ecuación (**53**).

$$V_o = G \cdot V_i = 0.5 \cdot V_i \tag{53}$$

Por último, para evitar desacoples indeseados a la entrada del TCA785 se ha colocado otro buffer de ganancia unitaria correspondiente a la ecuación (**54**).

$$V_o = G \cdot V_i = V_i \tag{54}$$

Las configuraciones de estas etapas están en la tabla (**Tabla 18**) y la figura (**Fig. 33**).

Tabla 18 *Componentes de la etapa sumadora y de desacoplo del regulador PI*

COMPONENTES	
Nombre	**Cantidad**
Resistor 10kΩ	4
TL081	2
AD623	1

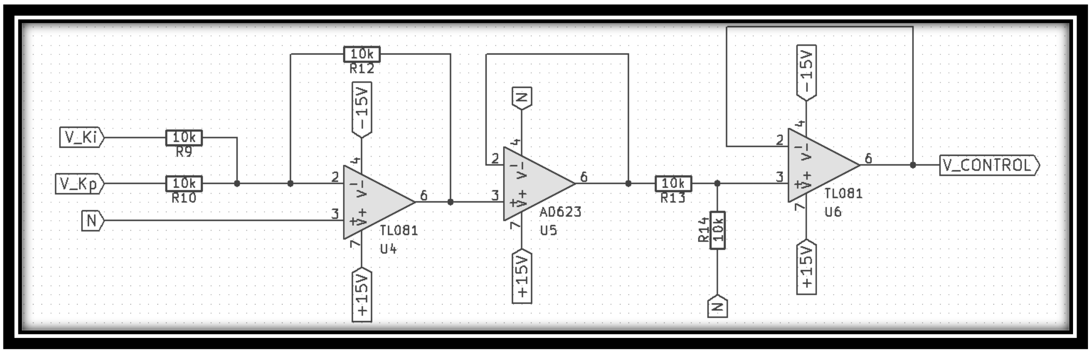

Fig. 33 *Esquemático de la etapa sumadora y de desacoplo del regulador PI*

11 PLACA DE CIRCUITOS IMPRESOS

Para materializar el control de velocidad del motor, se han realizado tres placas de circuitos impresos independientes.

1. PCB de alimentación
2. PCB de control
3. PCB de potencia

El tamaño de cada placa de circuitos impresos es de 10 cm de ancho por 15 cm de largo. Como software de diseño se ha empleado *Proteus 8 Profesional*.

11.1 PCB de alimentación

En esta placa se encuentran los transformadores de la etapa de control y los reguladores de tensión (con su rectificador y filtro). Esta placa se conecta a la PCB de control por medio de un cable de pines hembra. Su función es la de alimentar todos los circuitos integrados de la etapa de control. Las señales de sincronismo de los TCA785 también están incluidas en esta PCB.

La tabla (**Tabla 19**) y la figura (**Fig. 34**) muestran los componentes y el layout de la placa de circuitos impresos.

Tabla 19 Componentes de la PCB de alimentación

COMPONENTES	
Nombre	**Cantidad**
Transformadores FS28-1300-C2	2
1N4007	5
C2700uF25V	5
7815	4
7915	1
C300nF	5
1N4007	5
Resistor 10kΩ	3
Conector DIL-10	1
Conector TBLOCK-I4	1

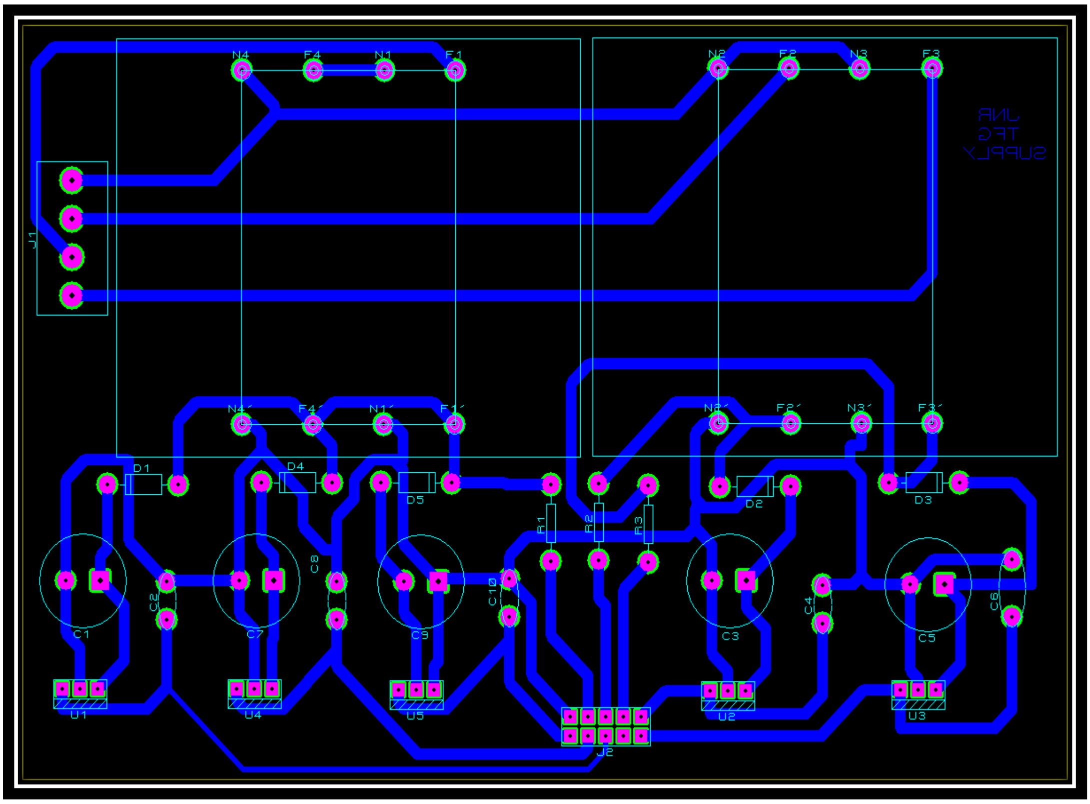

Fig. 34 Layout de la PCB de alimentación

11.2 PCB de control

En esta placa se encuentran todos los componentes relacionados con el control de fase y el regulador PI analógico del motor R3L. Su función es generar los pulsos necesarios para el control de fase de los tiristores y generar una tensión de control en función de una referencia fijada por el usuario y por la tensión obtenida por la tacodinamo. Esta PCB también es de 10x15 cm, la única diferencia es que está realizada a doble capa.

La tabla (**Tabla 20**) y la figura (**Fig. 35**) muestran los componentes y el layout de la placa de circuitos impresos.

COMPONENTES	
Nombre	**Cantidad**
TCA785	3
555	3
Transformadores SKPT 25b3	6
TL081	5
AD623	1
1N4148	12
Resistencia 10k	14
Resistencia 100	6
Resistencia 55k	3
Resistencia 47k	3
Resistencia 3K9	3
Resistencia 3K	3
Capacitor 47n	3
Capacitor 150n	6
Capacitor 1u	1
Capacitor 68n	3
Conector DIL-10	1
Conector DIL-14	1

Tabla 20 Componentes de la PCB de control

COMPONENTES	
Nombre	**Cantidad**
TCA785	3
555	3
Transformadores SKPT 25b3	6
TL081	5
AD623	1
1N4148	12
Resistencia 10k	14
Resistencia 100	6
Resistencia 55k	3
Resistencia 47k	3
Resistencia 3K9	3
Resistencia 3K	3
Capacitor 47n	3
Capacitor 150n	6
Capacitor 1u	1
Capacitor 68n	3
Conector DIL-10	1
Conector DIL-14	1

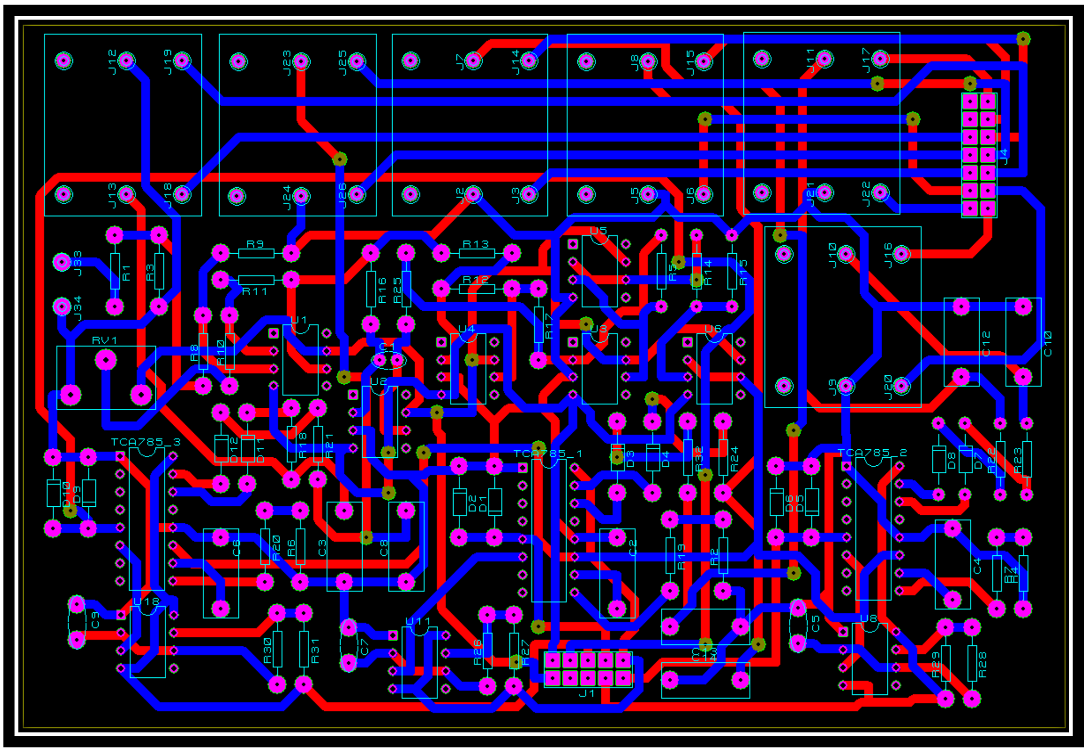

Fig. 35 *Layout de la PCB de control*

11.3 PCB de potencia

En esta placa se encuentran los tiristores que realizarán la rectificación para alimentar el motor. Cuenta además con las resistencias limitadoras de corriente para evitar la destrucción de los SCR y conectores. A pesar de sus escasos componentes se ha realizado a dos capas y su tamaño es de 10x15.

La tabla (**Tabla 21**) y la figura (**Fig. 36**) muestran los componentes y el layout de la placa de circuitos impresos.

Tabla 21 *Componentes de la PCB de control*

COMPONENTES	
Nombre	**Cantidad**
BT151	6
Resistencia 820	6
Disipador T0-220	6
Conector DIL-14	1
Conector TBLOCK-I3	1
Conector TBLOCK-I4	1

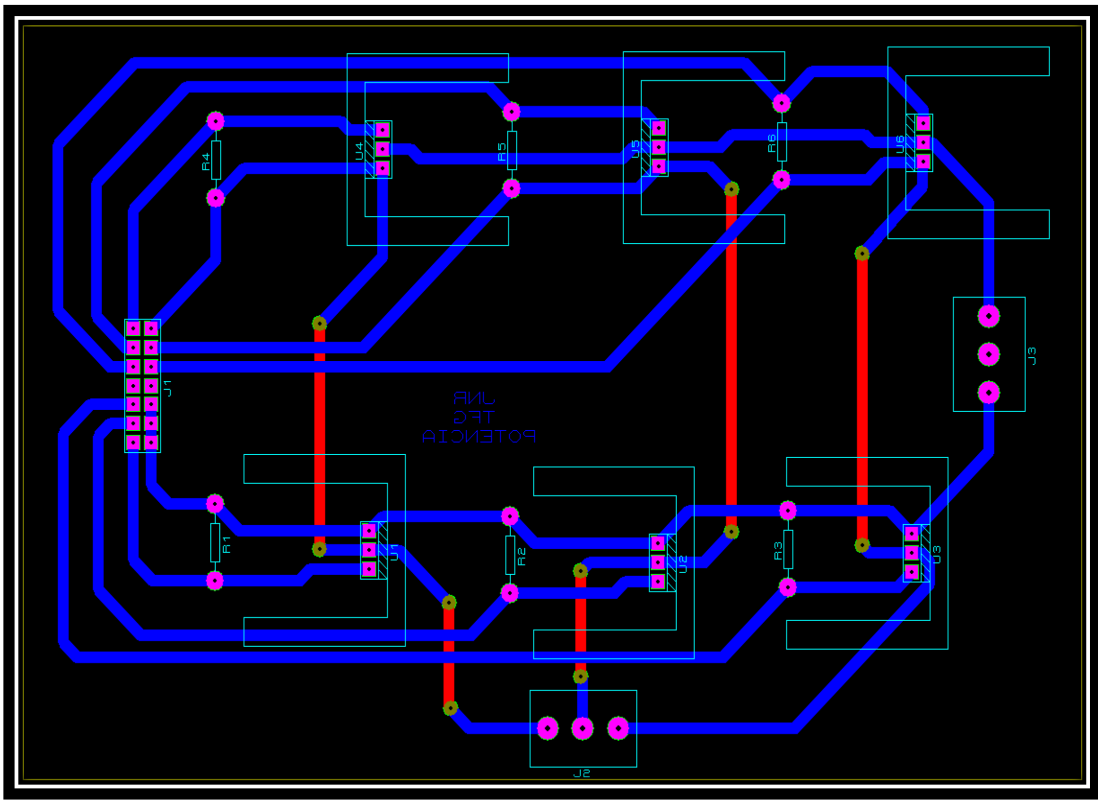

Fig. 36 *Layout de la PCB de potencia*

11.4 Fabricación y montaje de las pcb

11.4.1 Fabricación

Para la realización de las PCB se ha hecho uso del método de insolación y atacado mediante químicos.

Los materiales usados para la realización física de la PCB son los siguientes:

- Transparencia con las pistas del circuito.
- Placa fotosensible positiva.
- Insoladora.
- Liquido de revelado.
- Liquido atacante

El primer paso ha sido imprimir en fotolito las huellas de las pistas de las tres placas. Se ha exportado en formato BPM la capa correspondiente (Top copper o Bottom copper) del editor de PCB layout del *Proteus 8 Profesional*, la figura (**Fig. 37**) es un ejemplo. Comprobando que la escala es la correcta y que el dibujo de las pistas está en blanco y negro se ha impreso sobre el fotolito.

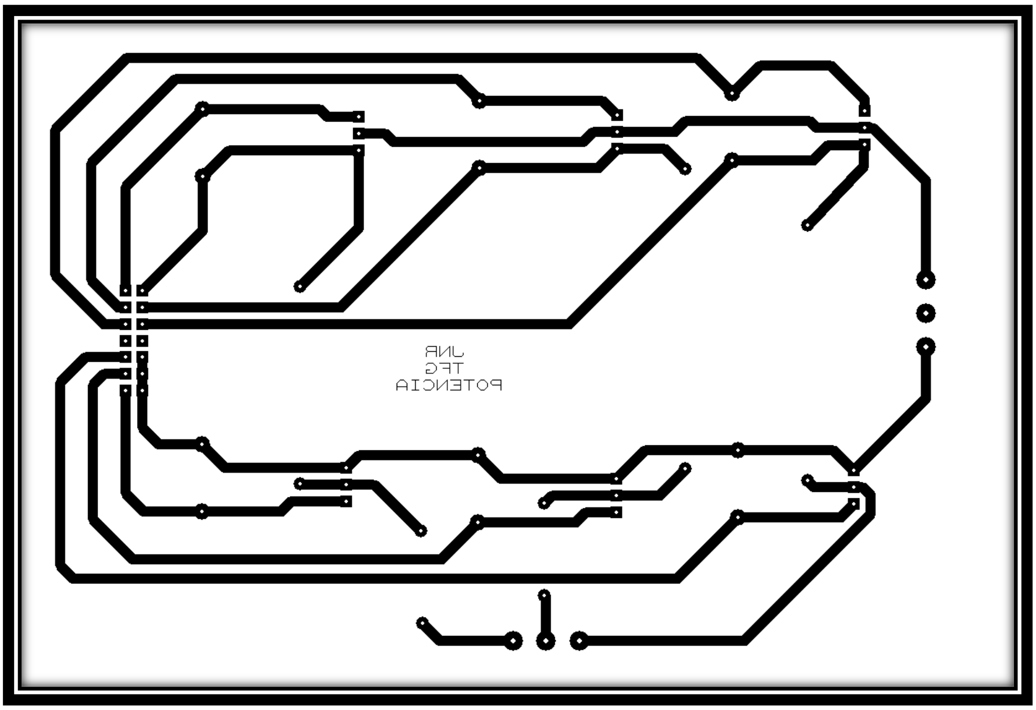

Fig. 37 *Huella de las pistas de una capa de la PCB de control a modo de ejemplo*

Las placas a usar son placas fotosensibles positivas. Estas placas traen protegida la cara o caras sensibles por una lámina ópaca para evitar que la luz natural las revele como se observa en la figura (**Fig. 38**). El tamaño es de 10x15 cm.

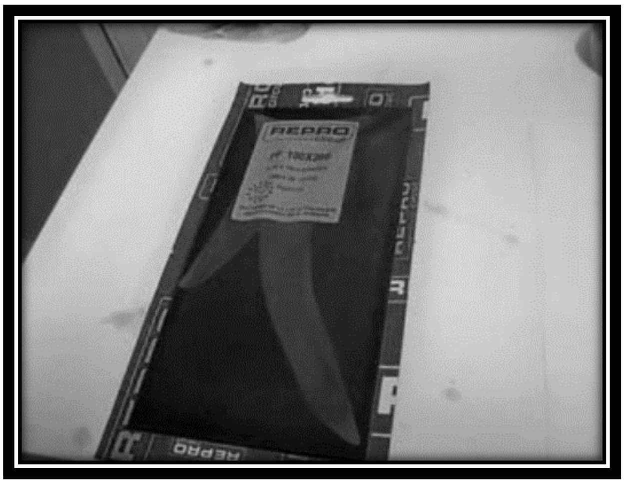

Fig. 38 *Placa fotosensible positiva cerrada*

La insoladora, mostrada en la figura (**Fig. 39**), es una fuente de luz ultravioleta que revela el fotolito sobre la placa fotosensible positiva. Para la insolación se ha retirado el film protector de la placa y se ha ajustado el fotolito encima de ella teniendo cuidado de no ponerla al revés. Se ha introducido varios minutos para su revelado.

__Fig. 39__ Insoladora para revelar las pistas sobre la placa fotosensible

Tras obtener el revelado de las pistas, se ha llevado sin ser expuesta a la luz natural a una zona donde poder realizar el atacado químico.

Primero se ha usado el líquido revelador (mezcla de agua y sosa cáustica). Se ha llenado una cubeta y se ha introducido la placa durante unos 10 minutos antes de introducirla en el líquido atacante.

El líquido atacante reacciona con el cobre, por lo tanto, no afectará a la zona de las pistas que se encuentran protegidas por el revelado del fotolito. Se balancea la bandeja con el líquido y la pcb dentro para realizar un atacado uniforme como muestra la figura (**Fig. 40**). Cuando se

__Fig. 40__ Atacado químico de las placas para eliminar el cobre sobrante

observa que se ha eliminado el cobre en su totalidad se enjuaga con agua y se limpia con alcohol la zona de las pistas para dejar al descubierto el cobre.

El resultado final, mostrado en la figura (**Fig. 41**), es una placa donde solo se observan las pistas deseadas en cobre.

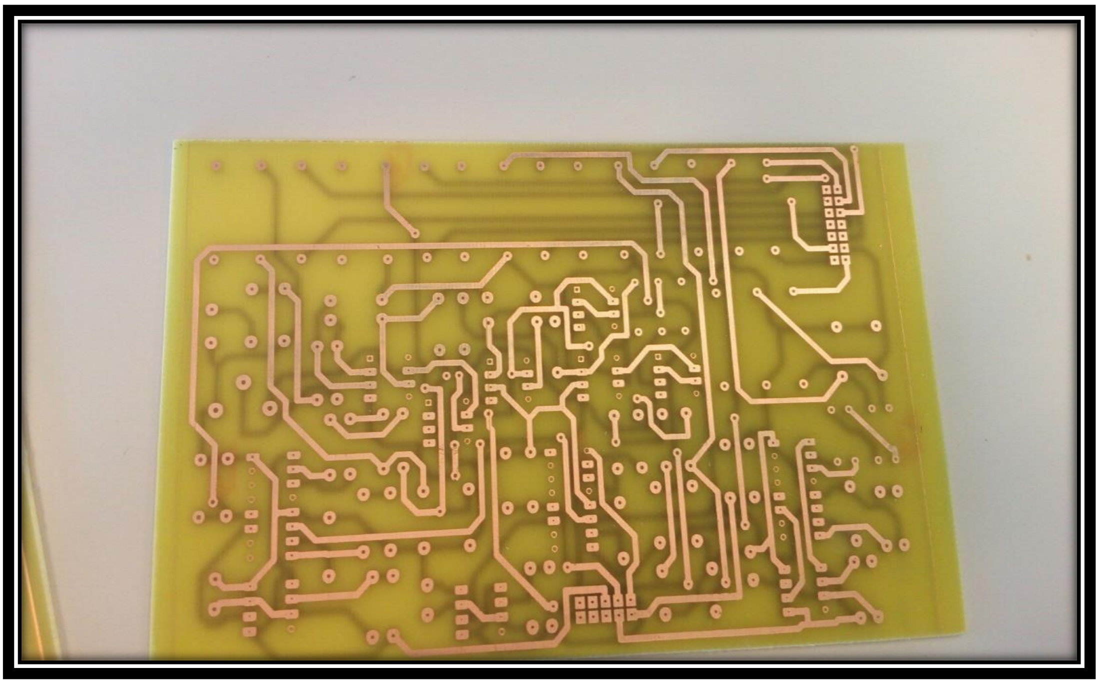

Fig. 41 *Pistas de cobre tras el atacado químico de la PCB de control*

11.4.2 Montaje

El primer paso ha sido perforar las placas. Para esto se ha hecho uso de brocas entre de 0.6mm y 1mm dependiendo del grosor del patillaje del componente. Se ha usado una taladradora

Fig. 42 *Dremel de banco usada para taladrar las PCB*

Dremel con banco de trabajo para realizar con precisión los agujeros como la de la figura (**Fig. 42**).

Por último, se han colocado los respectivos componentes y zócalos para su soldadura. Se ha soldado en una estación de soldadura con una temperatura de 200 ºC. Siendo el resultado final de una de las placas el mostrado por la figura (**Fig. 43**).

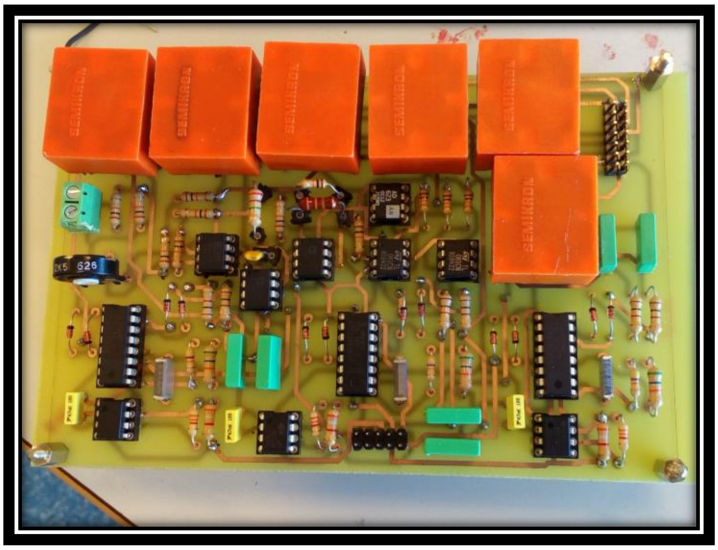

Fig. 43 *Resultado final de la placa de control*

Tras realizar el proceso para cada una de las placas, se han montado sobre torretas en cada una de sus esquinas y se ha conectado los cables que interconectan las tres PCBs como muestra la figura (**Fig. 44**).

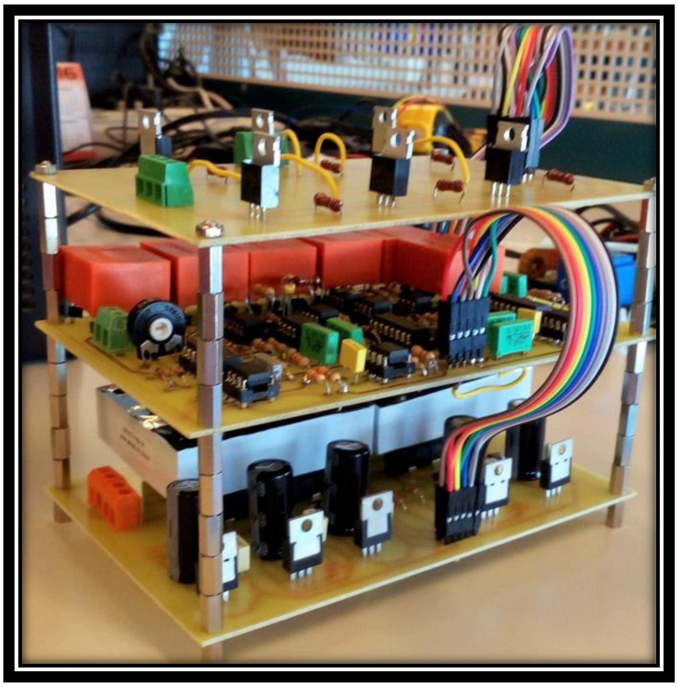

Fig. 44 *PCB de alimentación, control y potencia terminadas*

12 RESULTADOS

12.1 Señales de alimentación

Se ha comprobado que todas las alimentaciones sean correctas y no exista rizado alguno en ellas con los filtros que se han utilizado. Las tensiones a simular son las simétricas para la alimentación de los amplificadores operacionales del regulador PI y las tensiones de alimentación de cada TCA785. Los resultados se observan en la figura (Fig. 45)

Fig. 45 *Tensiones de alimentación de los TCA785 y el regulador PI*

Se comprueba así que no existe rizado alguno en las señales de alimentación. De ser así, podría afectar, por ejemplo, a las señales generadas por los TCA785 o los 555, ya que éstas dependen de la tensión de alimentación.

12.2 Señales de disparo de los tiristores

Se comprueba que están desfasadas entre sí 120º y sincronizadas con la tensión de rampa (ésta está sincronizada con los pasos por 0 de la tensión de sincronismo). Además de comprobar que los CI555 están realizando correctamente el troceado de la señal de salida al activar y desactivar la entrada de inhibición del TCA785.

12.2.1 Ángulo de disparo α=0º

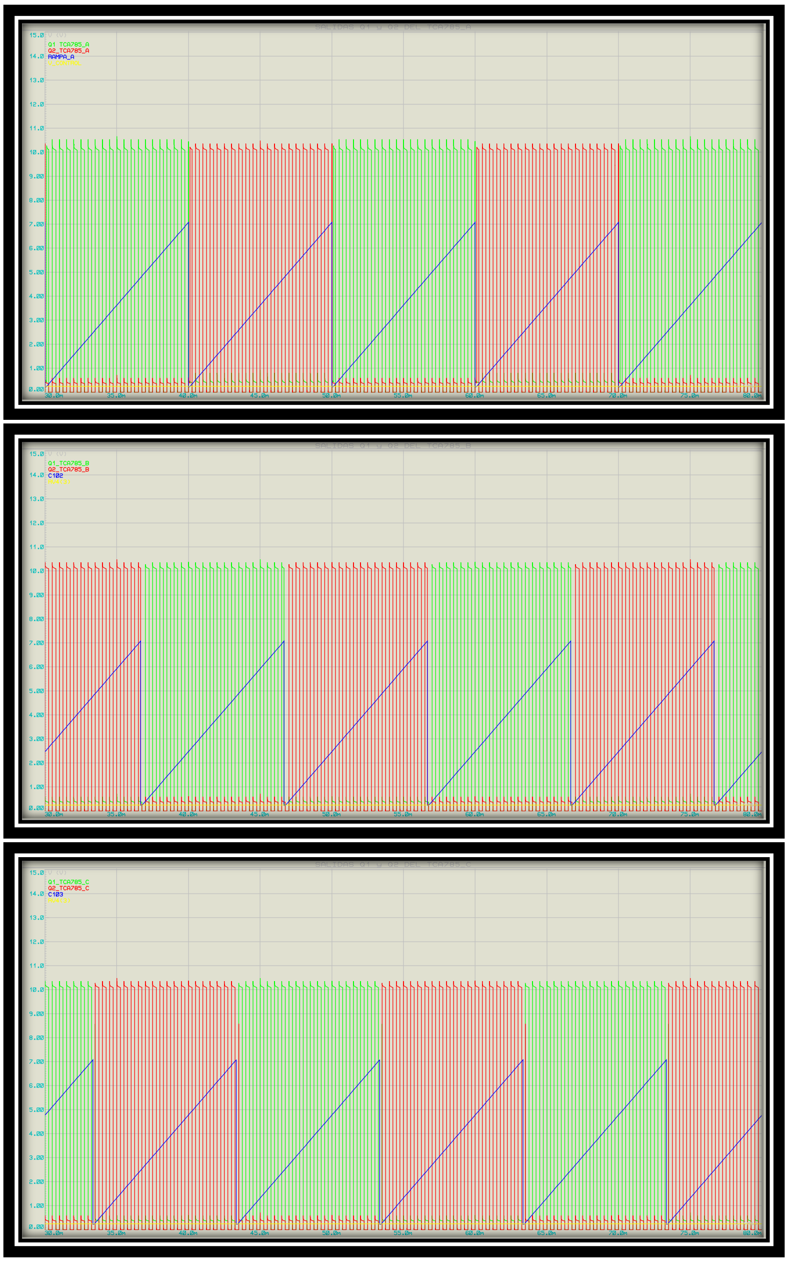

Fig. 46 *Salidas Q1 y Q2 de los TCA785, rampa y tensión de control a ángulo de disparo 0 grados*

12.2.2 Ángulo de disparo α=45º

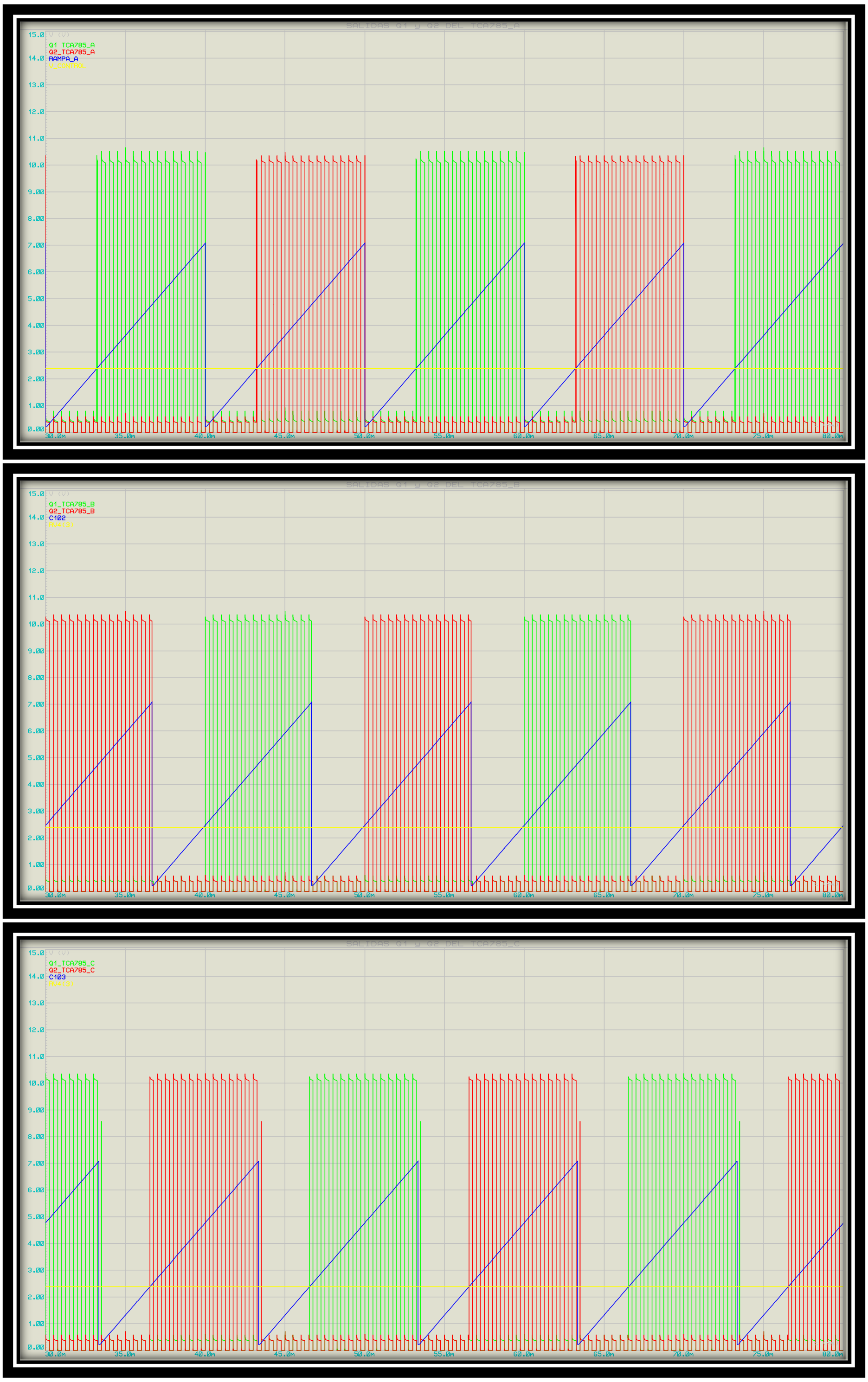

Fig. 47 Salidas Q1 y Q2 de los TCA785, rampa y tensión de control a ángulo de disparo 45 grados

12.2.3 Ángulo de disparo α=90º

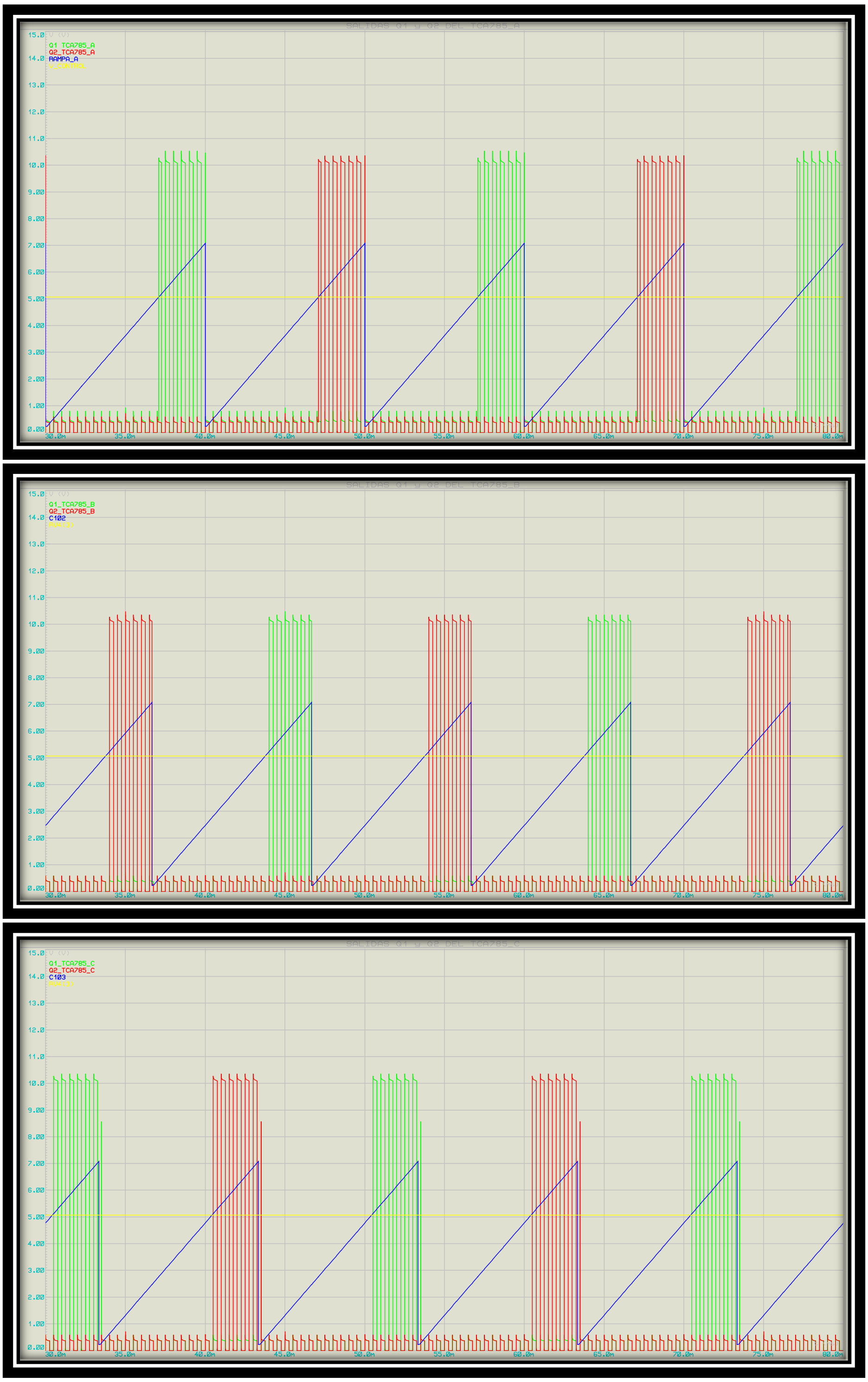

Fig. 48 *Salidas Q1 y Q2 de los TCA785, rampa y tensión de control a ángulo de disparo 90 grados*

12.2.4 Ángulo de disparo α=120º

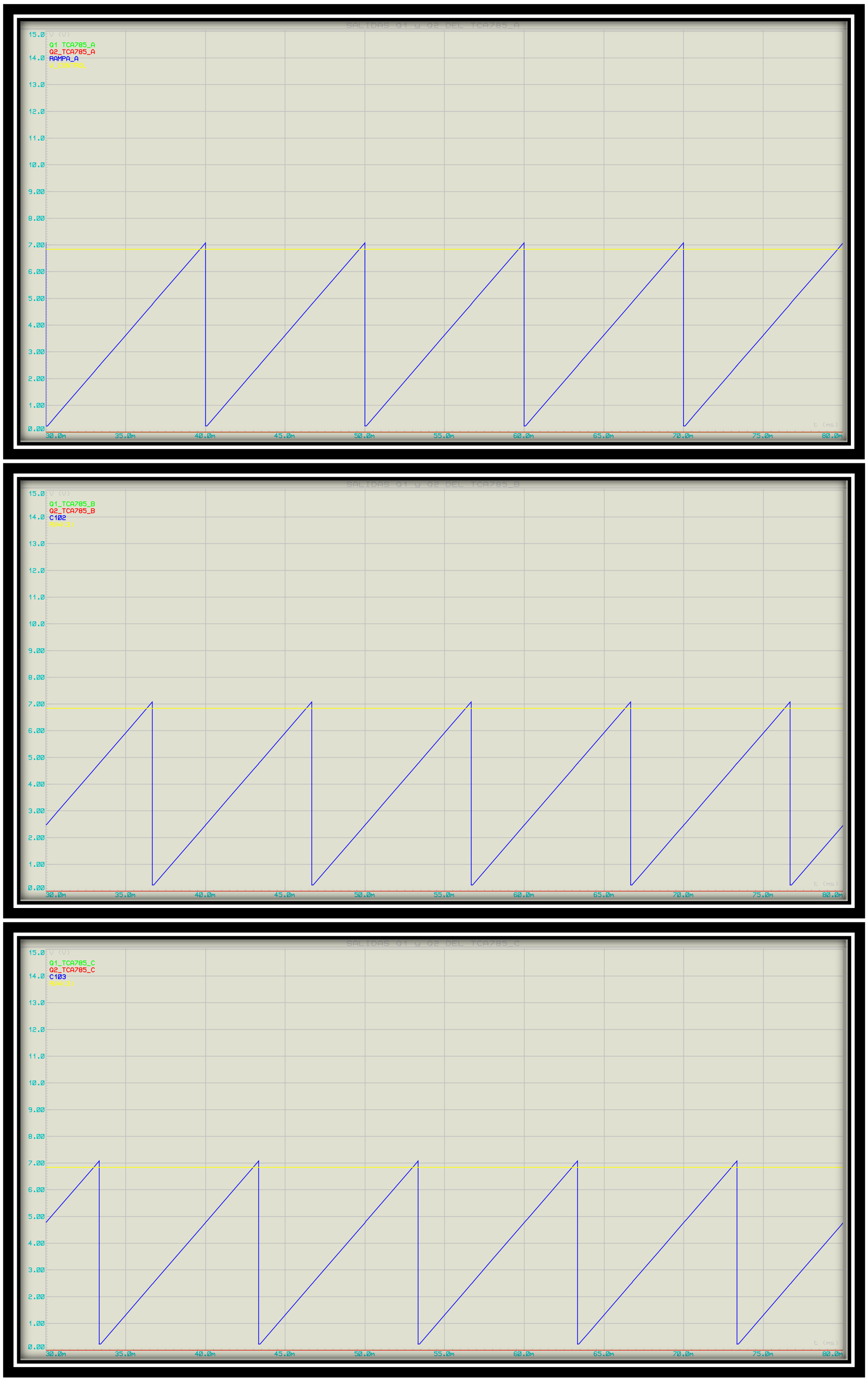

Fig. 49 Salidas Q1 y Q2 de los TCA785, rampa y tensión de control a ángulo de disparo 120 grados

12.3 Tensión de salida del rectificador trifásico

12.3.1 Ángulo de disparo α=0º

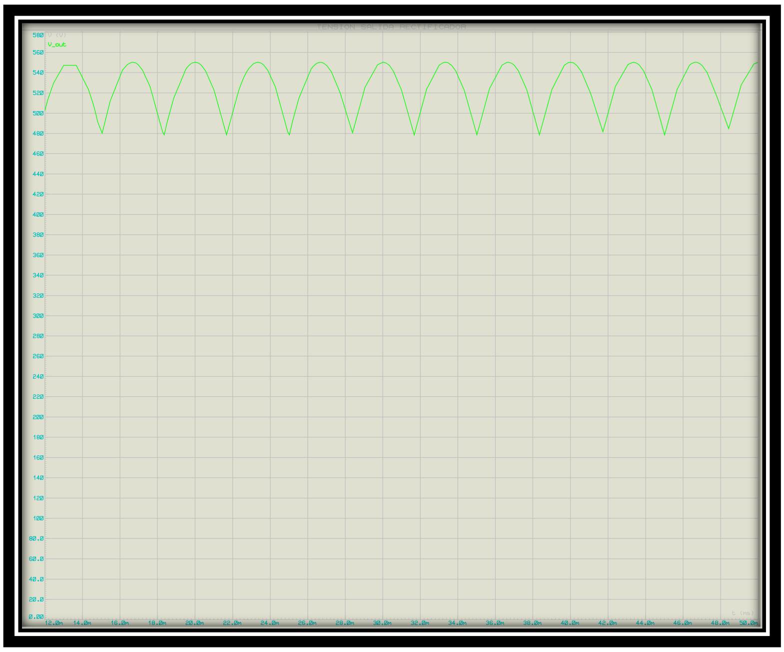

***Fig. 50** Tensión de salida del rectificador a ángulo de disparo 0 grados*

12.3.2 Ángulo de disparo α=45º

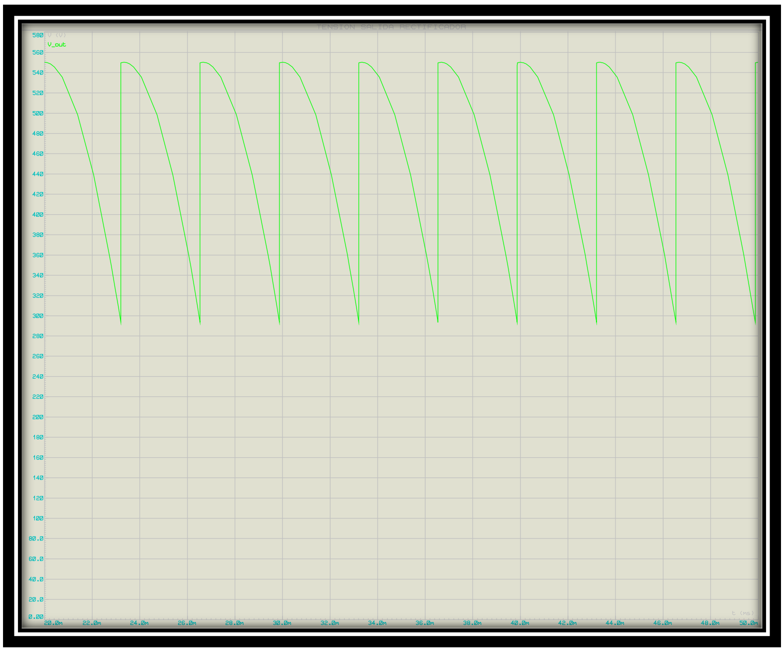

***Fig. 51** Tensión de salida del rectificador a ángulo de disparo 45 grados*

12.3.3 Ángulo de disparo α=90º

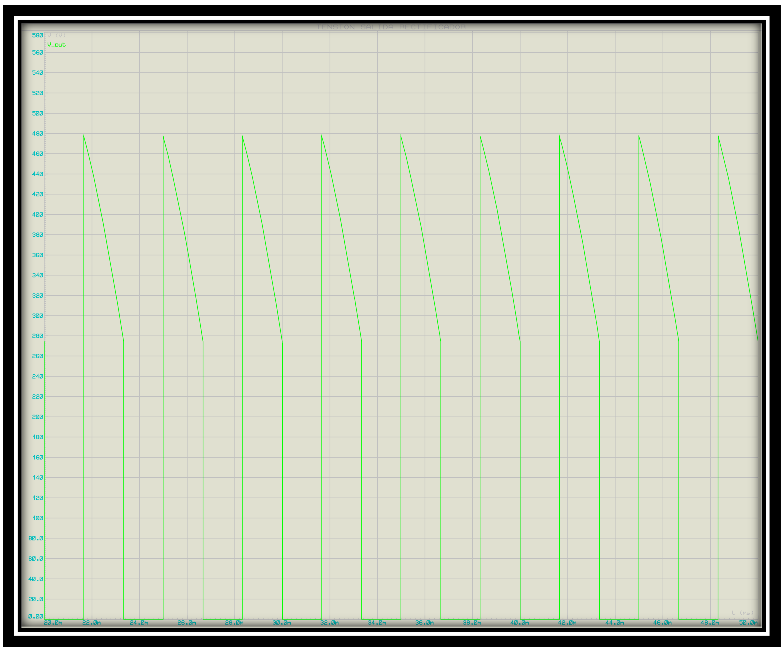

Fig. 52 Tensión de salida del rectificador a ángulo de disparo 90 grados

12.3.4 Ángulo de disparo α=120º

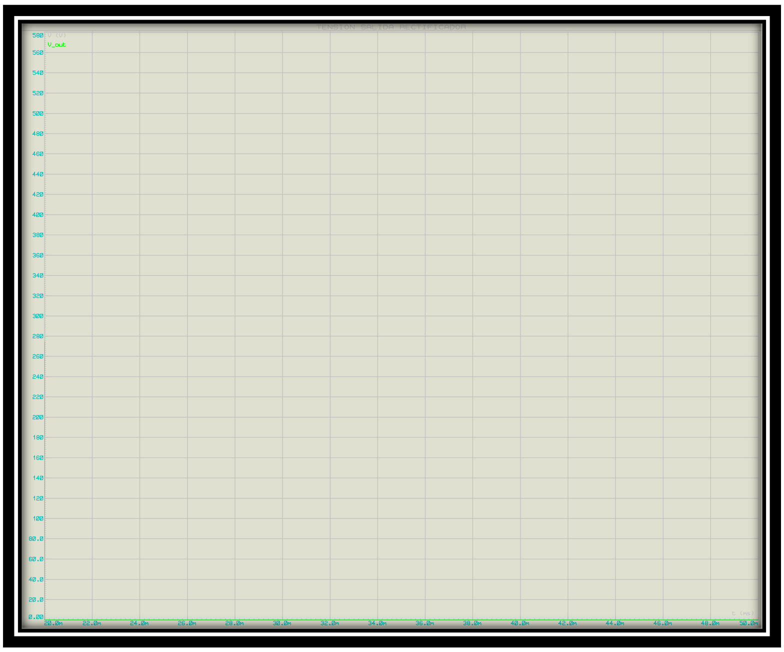

Fig. 53 Tensión de salida del rectificador a ángulo de disparo 120 grados

12.4 Regulador PI

La respuesta obtenida para los valores obtenidos por el PID tuner (Kp=1; Ki=100) puede observarse en la figura (**Fig. 54**). El tiempo de establecimiento al 95% es de 1.28s y el tiempo de subida es de 0.714s cumpliéndose así restricciones impuestas al sistema. Es decir, un tiempo de establecimiento al 95% menor de 2 segundos y un tiempo de subida menor de 1 segundo. Se observa además que la sobreoscilación ha desaparecido y que alcanza la referencia. En este caso de valor Vref= 1V por lo que la velocidad angular tiene que ser de 600 rpm.

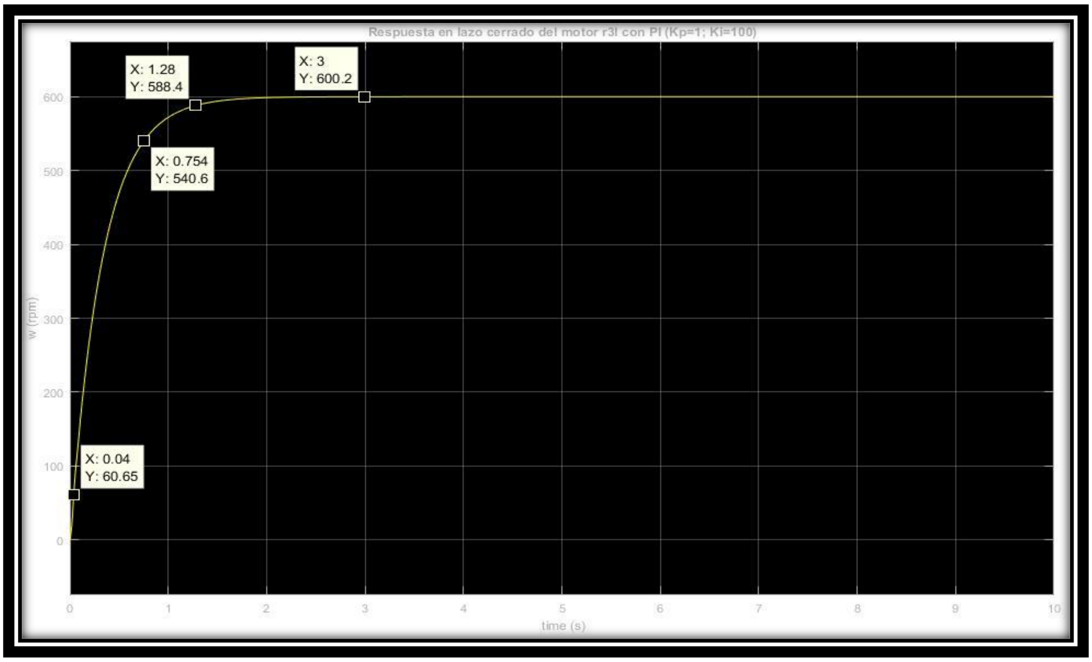

__Fig. 54__ Respuesta en lazo cerrado para Vref=1V; Kp=1; Ki=100

12.4.1 Respuesta en lazo cerrado para el rango de valores de Vref= [0,5] V

En la figura (**Fig. 55**) se observa como en todos los casos alcanza la referencia sin sobreoscilación en la velocidad correcta. El tiempo de establecimiento y de subida son aceptables en todos los casos.

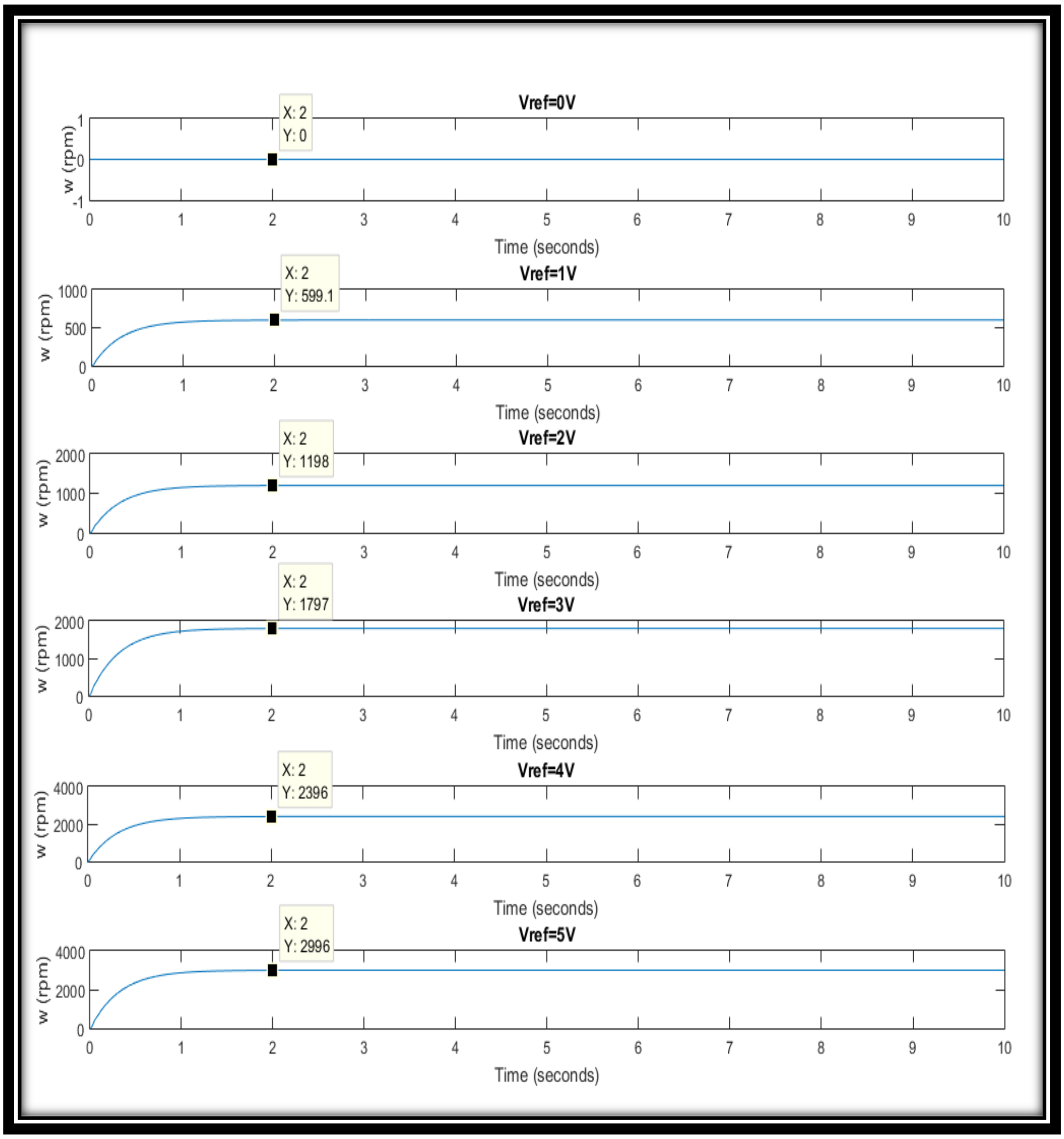

Fig. 55 *Respuesta en lazo cerrado para el rango de valores V=[0,5]*

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Universidad Politécnica de Valencia

Escuela Técnica Superior de Ingeniería del Diseño

Grado en Ingeniería Electrónica Industrial y Automática

Trabajo de Fin de Grado

IMPLEMENTACIÓN DE UN RECTIFICADOR TRIFÁSICO TOTALMENTE CONTROLADO Y CONTROL DE VELOCIDAD PARA MOTOR DC

II PLIEGO DE CONDICIONES

1 DEFINICIÓN Y ALCANCE

El objeto de este documento es determinar los requisitos mínimos del sistema de control de un de un motor de corriente continua, especificando las condiciones de durabilidad, fiabilidad y seguridad que debe cumplir. Como también describir con detalle las distintas partes que componen del sistema, determinar los documentos que serán de aplicación y definir las condiciones impuestas para puesta en marcha del sistema.

El alcance de aplicación de este documento abarca los distintos sistemas eléctricos y electrónicos que forman parte del sistema de control del horno, así como la instalación del mismo.

2 CONDICIONES Y NORMATIVAS

La normativa a respetar durante el desarrollo del proyecto es la siguiente:

- Directiva de Baja Tensión: Directiva 73/23/CEE del Consejo Europeo.
- Directiva 2002/95/CE del Parlamento y del Consejo Europeo, sobre las restricciones a la utilización de determinadas sustancias peligrosas en aparatos eléctricos y electrónicos.
- Directiva 2004/108/CE del Parlamento Europeo y del Consejo, de 15 de diciembre de 2004, relativa a la aproximación de las legislaciones de los Estados miembros en materia de compatibilidad electromagnética y por la que se deroga la Directiva 89/336/CEE.
- Directiva 2009/125/CE del Parlamento y del Consejo Europeo, por la que se instaura un marco para el establecimiento de requisitos de diseño ecológico aplicables a los productos que utilizan energía y por la que se modifica la Directiva 92/42/CEE del Consejo y las Directivas 96/57/CE y 2000/55/CE del Parlamento Europeo y del Consejo.
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- UNE-EN 60249-2-3:2001. Materiales base para circuitos impresos. Parte2: especificaciones. Sección3: papel celuloso con resina episódica, laminado con cobre, de inflamabilidad definida (ensayo de combustión vertical).

3 CONDICIONES FUNCIONALES

A continuación, se muestran las condiciones técnicas particulares que deben cumplir los distintos componentes utilizados para el desarrollo del proyecto.

3.1 Transformador FS28-1300-C2

***Tabla 22** Condiciones funcionales transformador FS28-1300-C2*

Potencia máxima	36VA
Voltaje en el devanado primario	230V en serie; 115V en paralelo
Voltaje máximo entre devanados	Hasta 300V
Frecuencia	50/60 Hz
Dimensiones	3,97x5,65x6,67cm
Peso	498g

3.2 Transformador SKPT 25b3

***Tabla 23** Condiciones funcionales transformador SKPT 25b3*

Potencia máxima	2VA
Aislamiento galvánico	4000V
Voltaje máximo entre devanados	Hasta 500V
Corriente máxima en el primario	300A
Corriente máxima en el secundario	0.3A
Dimensiones	1.51x2.71x2.33cm
Peso	63g

3.3 TCA785

***Tabla 24** Condiciones funcionales TCA785*

Potencia máxima	6VA
Voltaje de alimentación (recomendado)	8-18V
Tj máximo	150 ºC
Frecuencia	10-500Hz
Dimensiones	1.78x0.77cm
Peso	19g

3.4 555

***Tabla 25** Condiciones funcionales 555*

Potencia máxima	0.225VA
Voltaje de funcionamiento	4.5-16V
Corriente de funcionamiento	10-15mA
Temperatura de operación	0-75 ºC
Dimensiones	0.77x0.77cm
Peso	2g

3.5 TL081

Tabla 26 *Condiciones funcionales TL081*

Potencia máxima	50.4mVA
Voltaje de funcionamiento	5-15V
Voltaje diferencial	±30V
Temperatura de operaciónl	-55 -125 ºC
Tj máximop	150 ºC
Slew rate	8-13 V/us
Dimensiones	0.77x0.77cm
Peso	3g

3.6 AD623 Single Supply

Tabla 27 *Condiciones funcionales AD623 en Single Supply*

Potencia máxima	8.25mVA
+Vcc	3-12V
-Vcc	0V
Tensión de offset a la salida	200-1000uV
Slew Rate	0.3V/us
Temperatura de operación	-40 -85 ºC
Dimensiones	0.77x0.77cm
Peso	3g

3.7 BT151 650R

Tabla 28 *Condiciones funcionales BT151 650R*

Voltaje de pico en no-conducción	650V
Corriente media en conducción	7.5A
Corriente eficaz en conducción	12A
Corriente de pico en conducción	100A
Corriente de pico de puerta	2A
Tensión de pico de puerta	5V
Potencia de pico de puerta	5W
Tj máximo	125 ºC
Corriente de puerta	2-15mA
Corriente de mantenimiento	7-20Ma
Dimensiones	2.84x1.01x0.3cm
Peso	2g

4 MONTAJE VERTICAL

Dado que las PCB’s cuentan soldaduras en la parte inferior (en el caso de una capa) o ambas (en el caso de dos capas) es necesario su montaje sobre soportes. El soporte seleccionado son torretas enroscables de diámetro 0.8mm.

Las PCB’s son de igual tamaño (100x150mm). Es necesario un taladro del diámetro elegido para perforar de forma equidistante las placas de circuitos impresos.

Las torretas se enroscan una encima de otra hasta obtener una altura que no entorpezca los circuitos de ninguna de las placas y que permita la correcta ventilación de los mismos.

5 CONDICIONES FACULTATIVAS

Las condiciones que debe cumplir el proyectista son las siguientes:

- Conocer la normativa y aplicarla en todos los ámbitos del proyecto.
- Conocer las partes del proyecto en su totalidad.
- Cumplir con los plazos especificados.
- Notificación del inicio y finalización de las partes realizadas incluyendo pruebas.
- Cumplir con los protocolos de seguridad.

Las condiciones que el contratista debe cumplir son las siguientes

- Recibir la remuneración acordada entre proyectista y contratista.

6 CONDICIONES LEGALES

- Reponer todos aquellos materiales o trabajos que no se ajusten a las calidades especificadas en el proyecto.
- Durante la ejecución del proyecto se adoptarán las medidas necesarias de seguridad para evitar cualquier tipo de accidente y se cumplirá la normativa vigente en cuanto a seguridad e higiene en el trabajo.
- La instalación eléctrica deberá disponer de una toma de tierra de acuerdo con la normativa del Reglamento Electrotécnica de Baja Tensión.

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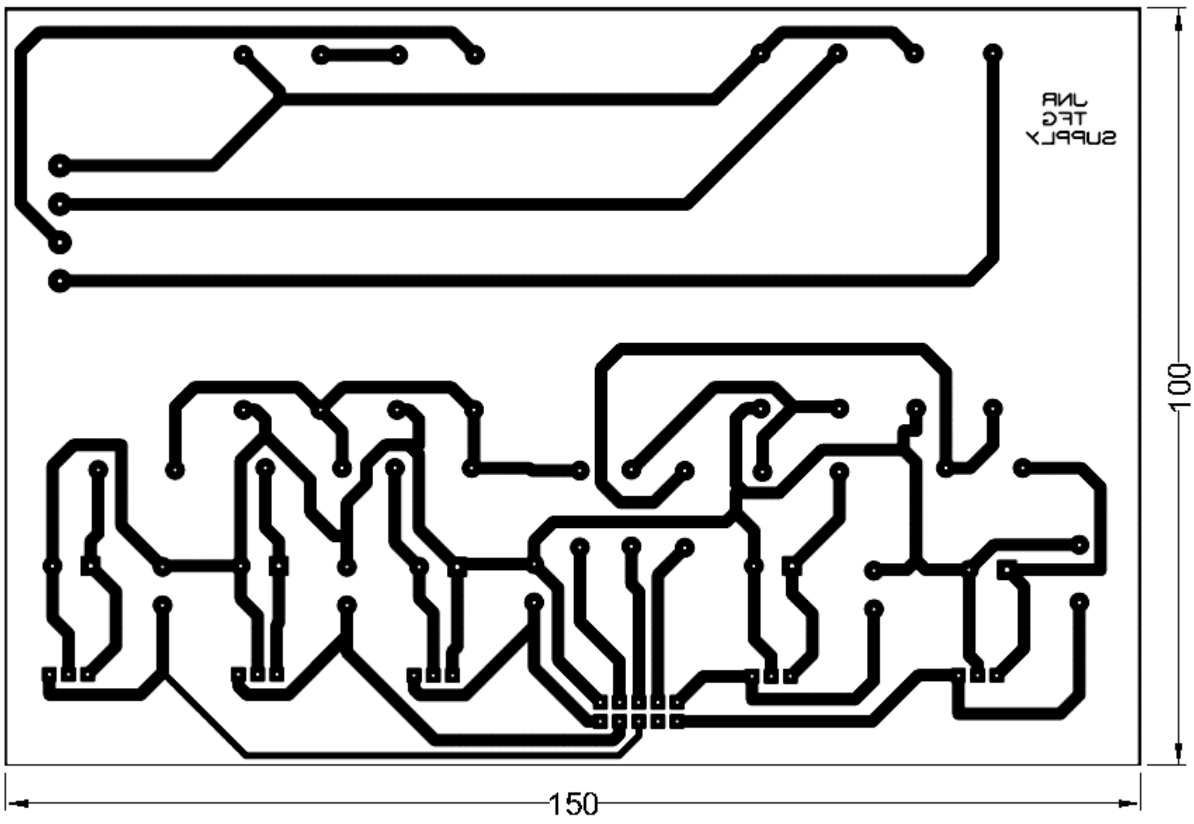
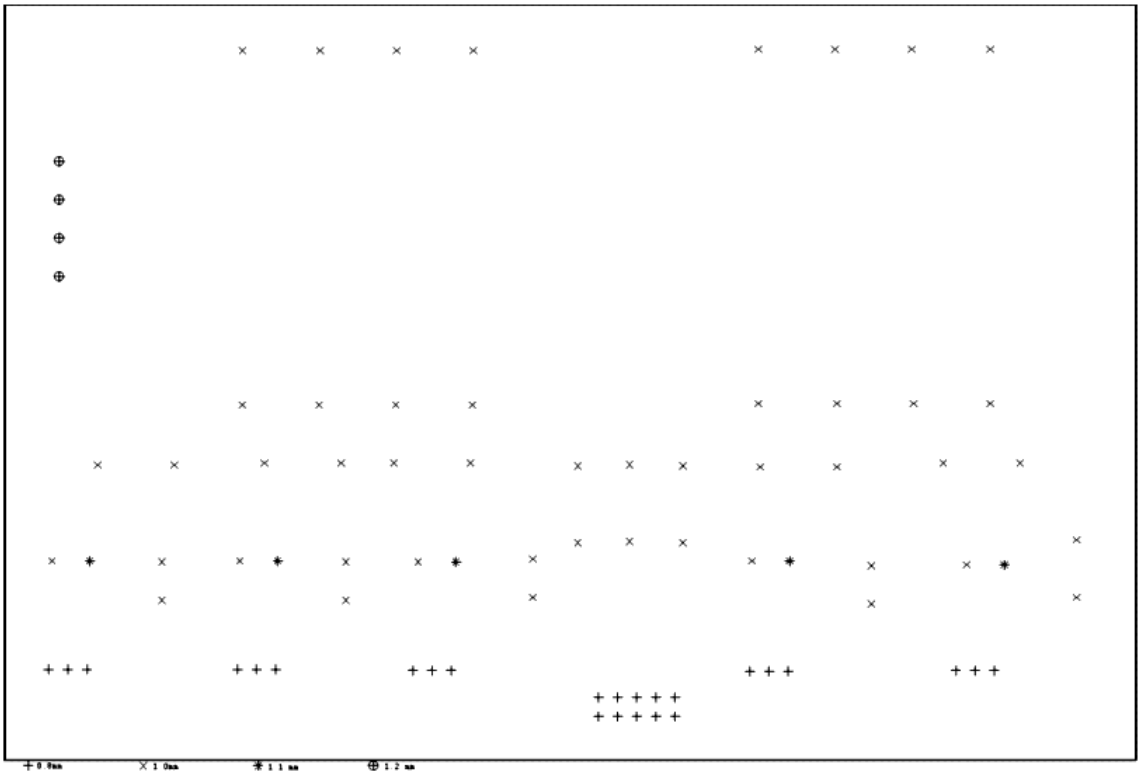
III PLANOS

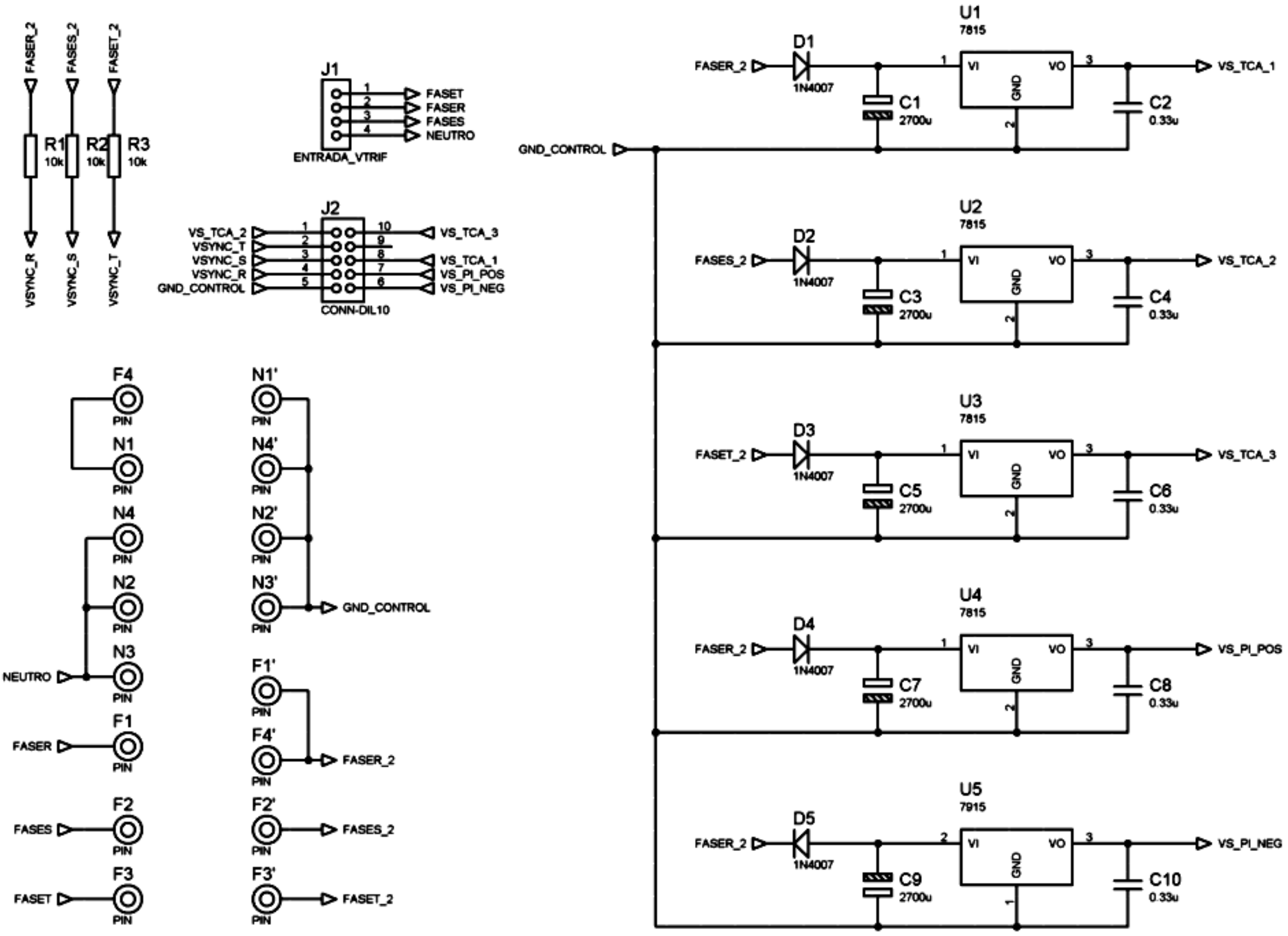
1 ÍNDICE DE PLANOS



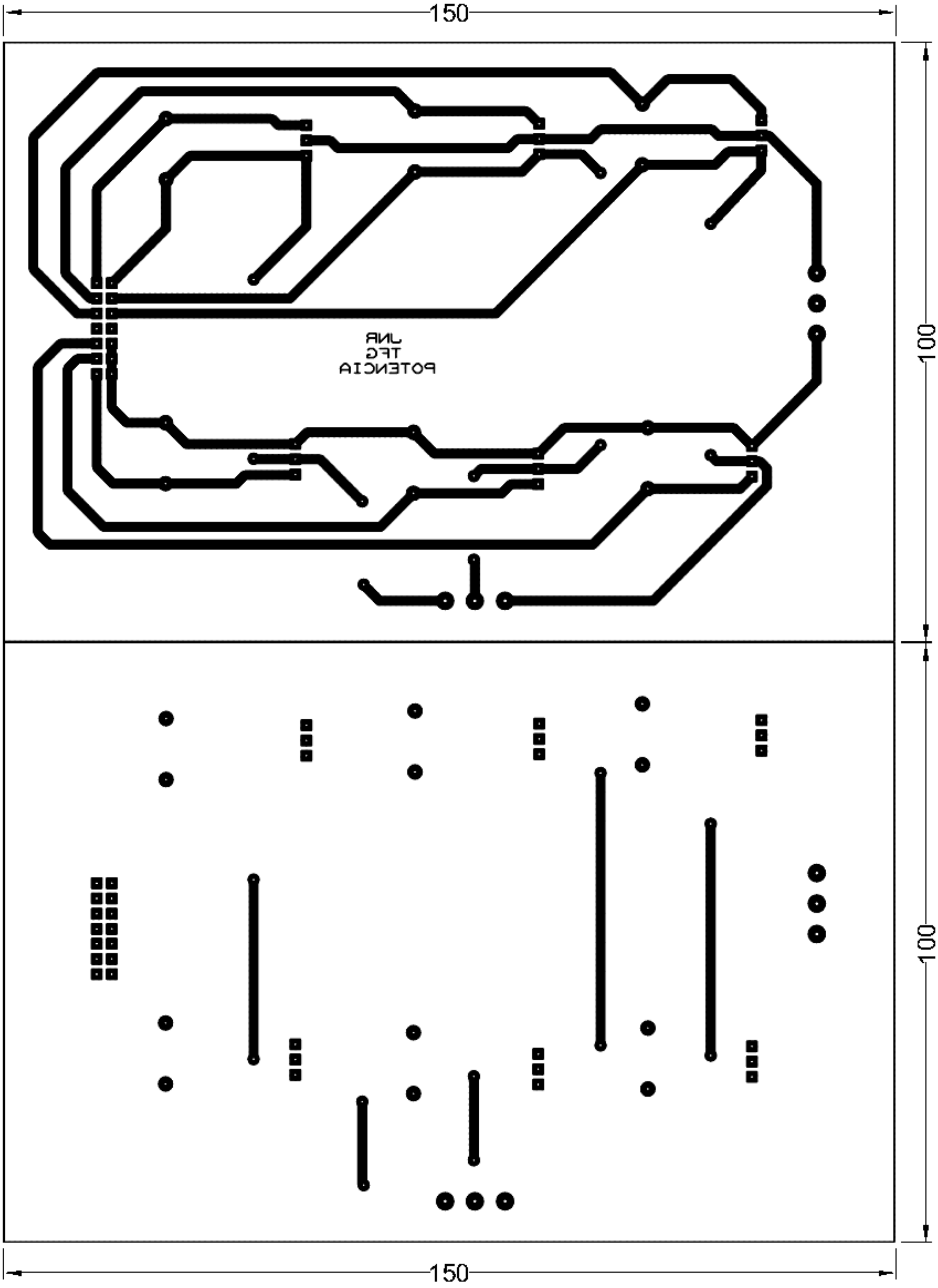
ESCALA	UNIDADES	NOMBRE DEL PLANO	
1:1	mm	PCB ALIMENTACIÓN	
Nº PLANO	FECHA	AUTOR	PROYECTO
1	8/30/16	Javier Novella Ruiz	Trabajo Final de Grado



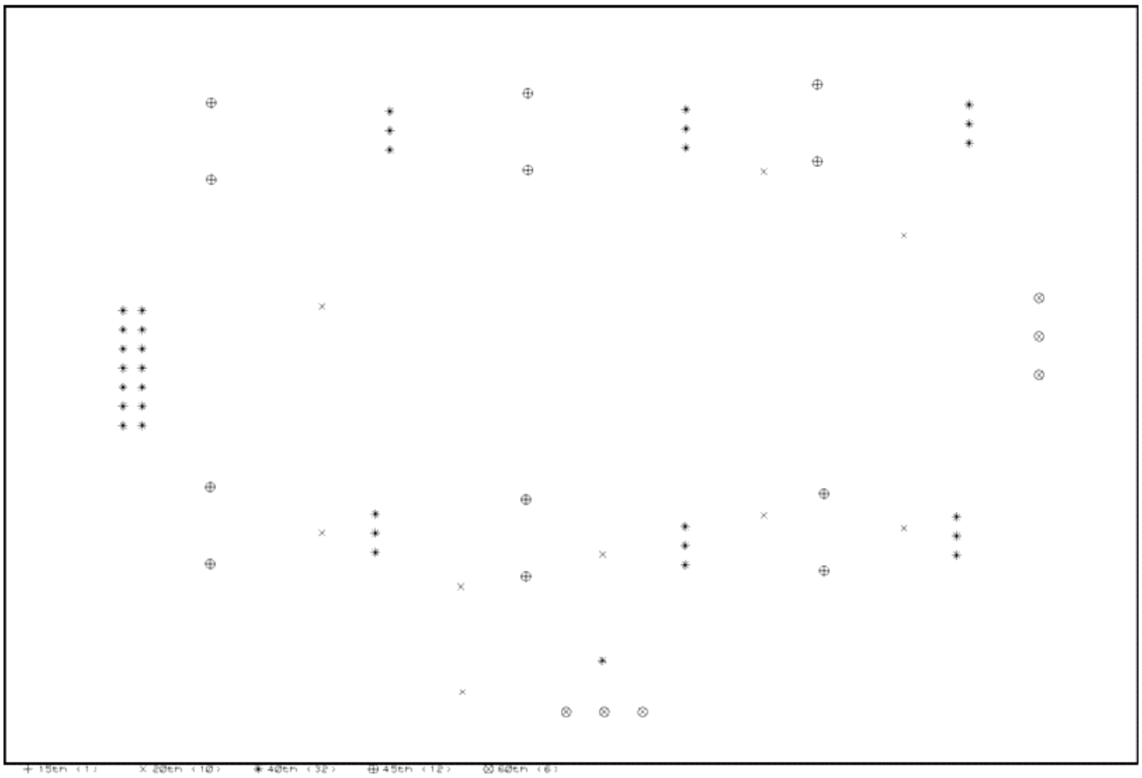
ESCALA	UNIDADES	NOMBRE DEL PLANO	
1:1	mm	TALADROS PCB ALIMENTACIÓN	
Nº PLANO	FECHA	AUTOR	PROYECTO
2	8/30/16	Javier Novella Ruiz	Trabajo Final de Grado



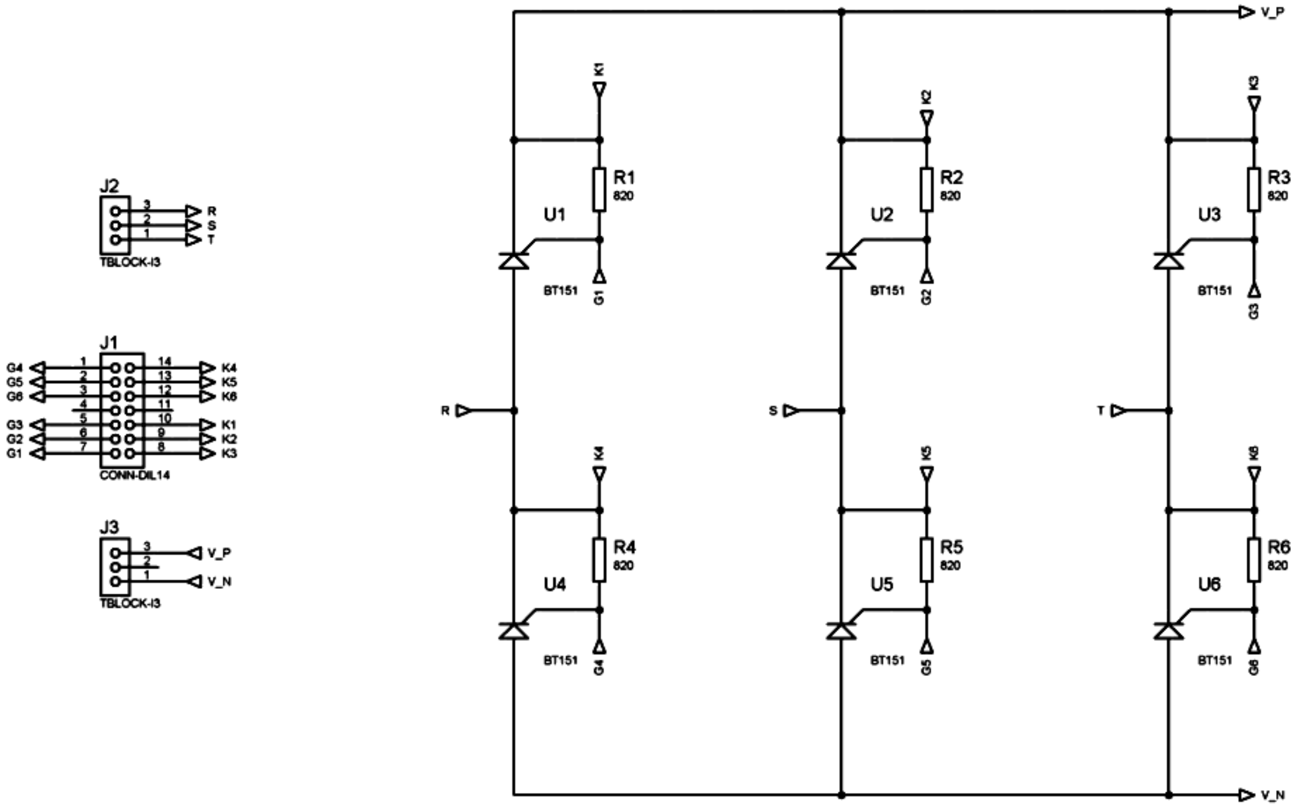
ESCALA	UNIDADES	NOMBRE DEL PLANO	
1:1	mm	ESQUEMÁTICO PCB ALIMENTACIÓN	
Nº PLANO	FECHA	AUTOR	PROYECTO
3	8/30/16	Javier Novella Ruiz	Trabajo Final de Grado



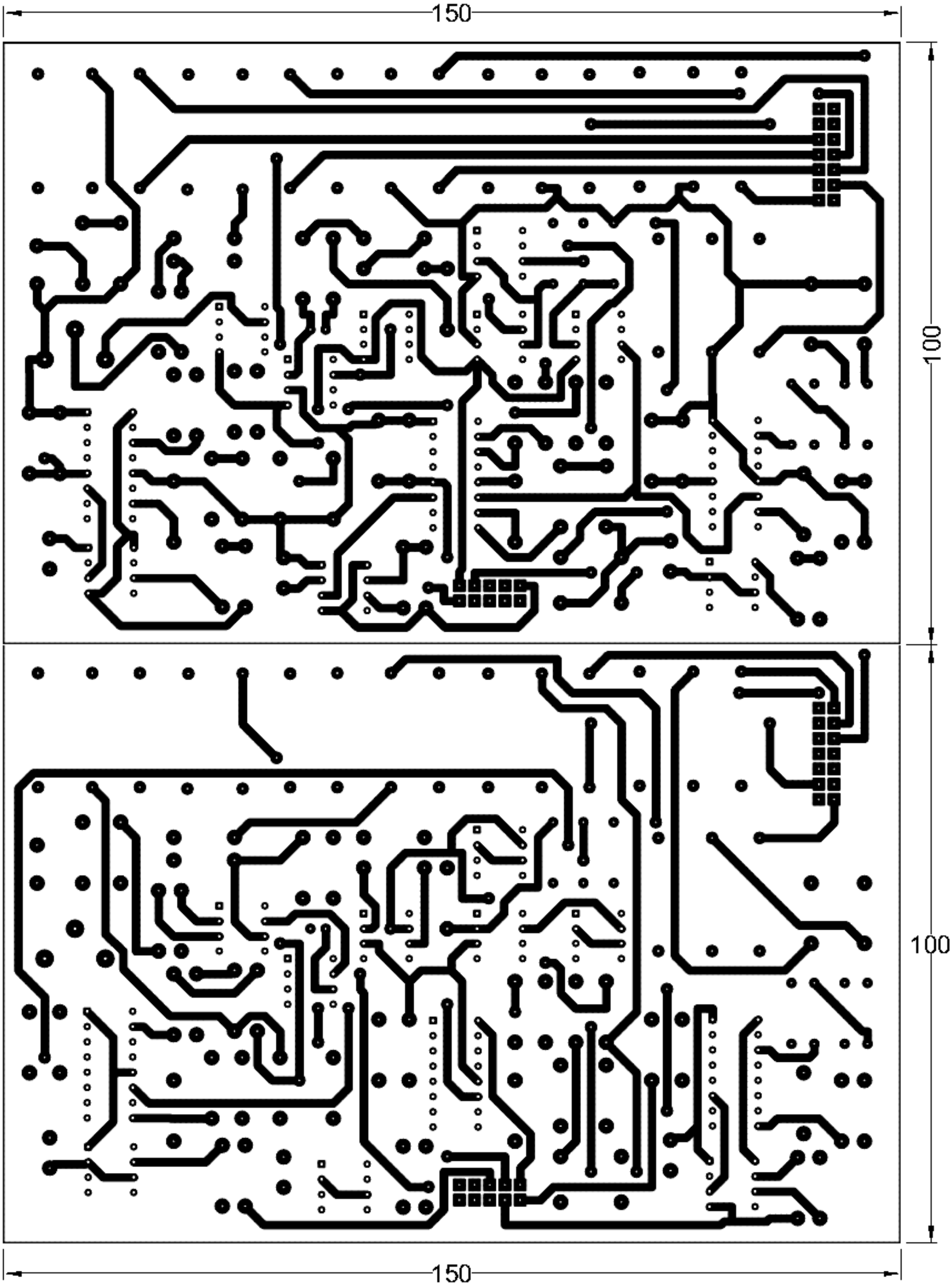
ESCALA	UNIDADES	NOMBRE DEL PLANO	
1:1	mm	PCB POTENCIA	
Nº PLANO	FECHA	AUTOR	PROYECTO
4	8/30/16	Javier Novella Ruiz	Trabajo Final de Grado



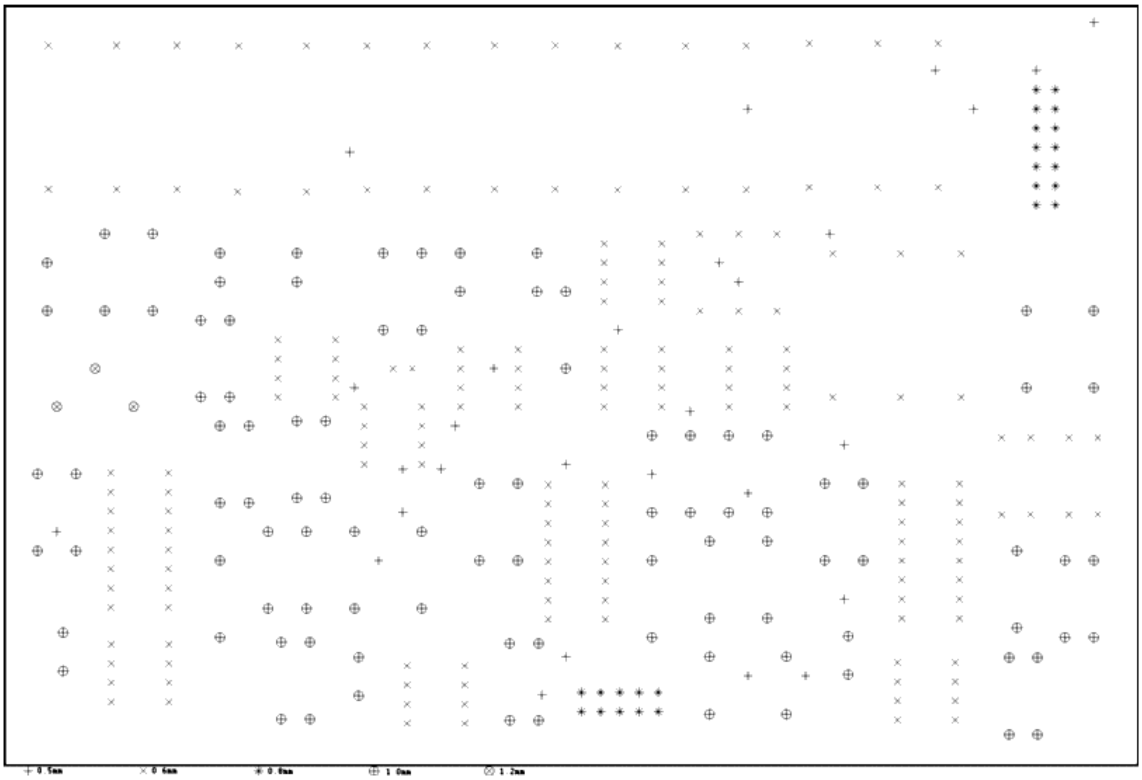
ESCALA	UNIDADES	NOMBRE DEL PLANO	
1:1	mm	TALADROS PCB POTENCIA	
Nº PLANO	FECHA	AUTOR	PROYECTO
5	8/30/16	Javier Novella Ruiz	Trabajo Final de Grado



ESCALA	UNIDADES	NOMBRE DEL PLANO	
1:1	mm	ESQUEMÁTICO PCB POTENCIA	
Nº PLANO	FECHA	AUTOR	PROYECTO
6	8/30/16	Javier Novella Ruiz	Trabajo Final de Grado

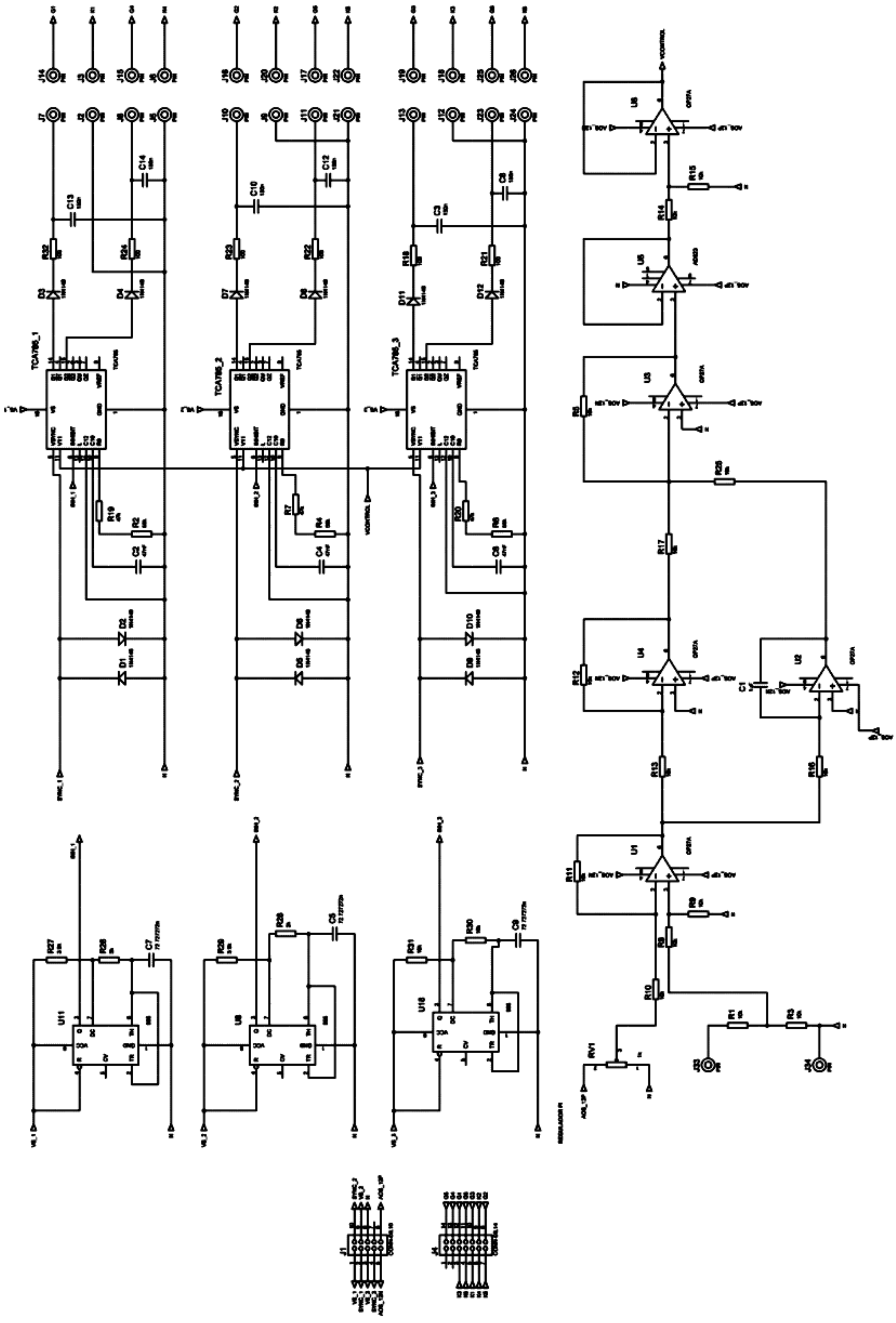


ESCALA	UNIDADES	NOMBRE DEL PLANO	
1:1	mm	PCB CONTROL	
Nº PLANO	FECHA	AUTOR	PROYECTO
7	8/30/16	Javier Novella Ruiz	Trabajo Final de Grado



ESCALA	UNIDADES	NOMBRE DEL PLANO	
1:1	mm	TALADROS PCB CONTROL	
Nº PLANO	FECHA	AUTOR	PROYECTO
8	8/30/16	Javier Novella Ruiz	Trabajo Final de Grado

VNIVERSIDAD POLITECNICA VALENCIA



ESCALA	UNIDADES	NOMBRE DEL PLANO	
1:1	mm	ESQUEMATICO PCB CONTROL	
Nº PLANO	FECHA	AUTOR	PROYECTO
9	8/30/16	Javier Novella Ruiz	Trabajo Final de Grado

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IV PRESUPUESTO

***Tabla 29** Presupuesto PCB Alimentación*

Partida 1: PCB Alimentación

Encargado	Tiempo de fabricación	€/h	Total
Técnico	12	7,50	90,00 €
			90,00 €

Nombre	€/u	Unidades	Total
Transformador FS28-1300-C2	15,43	2	30,86 €
Diodo 1N4007	0,05	5	0,24 €
Condensador 2700u 25V	1,16	5	5,78 €
Condensador 330n	0,63	5	3,16 €
Regulador de tensión LM7815	0,55	4	2,21 €
Regulador de tensión LM7915	0,30	1	0,30 €
Resistencia 10k	0,04	3	0,12 €
Tira de pines 10 pin	0,77	1	0,77 €
Terminal para PCB tornillo 4 vías	1,32	1	1,32 €
Placa fotosensible positiva una cara 100x150	4,60	1	4,60 €
			49,36 €

Subtotal	139,36 €
Medios Auxiliares (2%)	2,79 €
Total	142,14 €

Tabla 30 *Presupuesto PCB Control*

Partida 2: PCB Control

Encargado	**Tiempo de fabricación**	**€/h**	**Total**
Técnico	16	7,50	120,00 €
			120,00 €

Nombre	**€/u**	**Unidades**	**Total**
Transformador SKPT25b3	5,03	5	25,15 €
Circuito integrado TCA785	6,26	3	18,78 €
Circuito integrado 555	1,82	3	5,46 €
Amplificador TL081	0,50	5	2,50 €
Amplificador AD623	4,63	1	4,63 €
Diodo 1N4148	0,10	12	1,20 €
Resistencia 10k	0,17	14	2,38 €
Resistencia 100	0,10	6	0,60 €
Resistencia 47k	0,17	3	0,51 €
Resistencia 3k9	0,30	3	0,90 €
Resistencia 3k	0,20	3	0,60 €
Resistencia 55k	0,23	3	0,69 €
Condensador 47n	1,34	3	4,02 €
Condensador 150n	0,66	6	3,96 €
Condensador 1u	1,26	1	1,26 €
Condensador 68n	1,32	3	3,95 €
Tira de pines 10 pin	0,77	3	2,31 €
Placa fotosensible positiva doble cara 100x150	5,56	1	5,56 €
			84,46 €

Subtotal	204,46 €
Medios Auxiliares (2%)	4,09 €
Total	208,55 €

Tabla 31 Presupuesto PCB Potencia

Partida 3: PCB Potencia

Encargado	**Tiempo de fabricación**	**€/h**	**Total**
Técnico	12	7,50	90,00 €
			90,00 €

Nombre	**€/u**	**Unidades**	**Total**
SCR BT151	0,65	6	3,90 €
Resistencia 820	0,17	6	1,02 €
Disipador TO-220	1,21	6	7,26 €
Tira de pines 10 pin	0,77	2	1,54 €
Terminal PCB tornillo 4 vías	1,32	1	1,32 €
Terminal PCB tornillo 3 vías	1,13	1	1,13 €
Placa fotosensible positiva doble cara 100x150	5,56	1	5,56 €
			21,73 €

Subtotal	111,73 €
Medios Auxiliares (2%)	2,23 €
Total	113,96 €

Tabla 32 Presupuesto Diseño del Proyecto

Partida 4: Diseño del proyecto

Encargado	**Tiempo de fabricación**	**€/h**	**Total**
Graduado en Ingeniería	300	11,50	3.450,00 €
			3.450,00 €

Subtotal	3.450,00 €
Medios Auxiliares (2%)	69,00 €
Total	3.519,00 €

Tabla 33 Presupuesto de la partida global del proyecto

Partida Global	
PCB Alimentación	142,14 €
PCB Control	208,55 €
PCB Potencia	113,96 €
Diseño del proyecto	3.519,00 €
Total del proyecto	3.983,65 €

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V ANEXO: DATASHEET

DATI MOTORE ***Motor ratings***	**SIMBOLI** ***Symbols***	**UNITÀ** ***Units***	**SERIE** ***Series*** **R3S**											
COPPIA ALLA VELOCITÀ NOMINALE *Torque at rated speed*	Cn	Nm	0.75	0.75	0.75				0.75	0.75	0.75			
VELOCITÀ NOMINALE *Rated speed*	Nm	RPM	2000	2000	2000				3000	3000	3000			
POTENZA NOMINALE *Reated output*	Pu	W	160	160	160				230	230	230			
TENSIONE NOMINALE *Rated Voltage*	Vn	V	170	48	24				170	48	24			
CORRENTE NOMINALE *Rated Current*	In	A	1.23	4.4	8.1				1.8	6.2	14			
COPPIA DI PICCO *Peak torque*	Cp	Nm	4.5	4.5	4.5				4.5	4.5	4.5			
CORRENTE DI PICCO *Peak current*	Ip	A	7.4	26.4	48.6				10.8	37.2	84			
RENDIMENTO *Efficiency*	-	%	78	76	76				77	77	73			
DATI MECCANICI *Mechanical data*														
INERZIA ROTORE *Rotor inertia*	J	Kg/m²	0.00057	0.00057	0.00057				0.00057	0.00057	0.00057			
MAX. ACCELLERAZ. TEORICA *Max theorical accelleration*	a	rad/ sec²	7900	7900	7900				7900	7900	7900			
CARICO ASSIALE MAX. *Max axial load*	Fa	N	119	119	119				119	119	119			
CARICO RADIALE MASSIMO *Max radial load*	Fr	N	480	480	480				480	480	480			
GRADO DI PROTEZIONE *Protection (IEC.34.5)*	-	IP	54	54	54				54	54	54			
PESO *Weight*	-	Kg	4.8	4.8	4.8				4.8	4.8	4.8			
DATI ELETTRICI *Winding data*														
COSTANTE DI TEMPO TERMICA *Thermal time constant*	Tt	min	90	90	90				90	90	90			
COSTANTE DI TEMPO ELETTRICA *Electrical time constant*	Te	ms	6.3	4	4.7				6.1	3.6	4.3			
RESISTENZA D'ARMATURA *Armature resistance*	Rm	Ohm	15.6	2.2	0.34				7.2	1.1	0.19			
INDUTTANZA D'ARMATURA *Armature inductance*	La	mH	98.5	7.5	1.6				47	4	0.81			
CLASSE ISOLAMENTO *Insulation class*	-	-	F	F	F				F	F	F			
FATTORE DI SERVIZIO *Duty*	-	-	S1	S1	S1				S1	S1	S1			
FATTORE DI FORMA *Form factor*	-	-	1	1	1				1	1	1.2			
TEMPERATURA AMBIENTE *Ambient temperature*	-	C°	25	25	25				25	25	25			
ALTEZZA *Height*	-	m	1000	1000	1000				1000	1000	1000			
TOLLERANZE *Tolerance*	-	%	+/-5	+/-5	+/-5				+/-5	+/-5	+/-5			

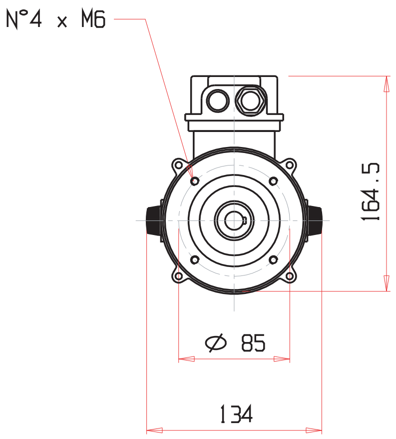
** Tensioni non a catalogo a richiesta
Not depliant voltage to request

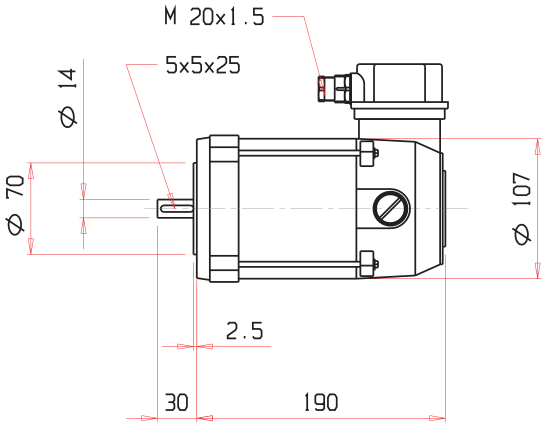
SERIE
Series

R3S

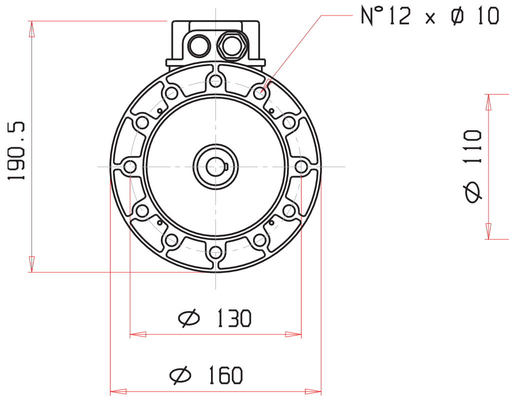
DIMENSIONI *Dimensions*

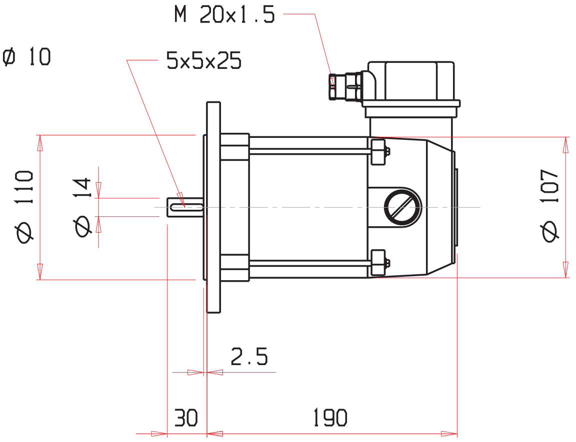
B14 M71





B5 M71





DATI MOTORE ***Motor ratings***	**SIMBOLI** ***Symbols***	**UNITÀ** ***Units***	**SERIE** ***Series*** **R3M**											
COPPIA ALLA VELOCITÀ NOMINALE *Torque at rated speed*	Cn	Nm	1.25	1.25					1.25	1.25				
VELOCITÀ NOMINALE *Rated speed*	Nm	RPM	2000	2000					3000	3000				
POTENZA NOMINALE *Reated output*	Pu	W	260	260					400	400				
TENSIONE NOMINALE *Rated Voltage*	Vn	V	170	48					170	48				
CORRENTE NOMINALE *Rated Current*	In	A	2.1	6.7					3	10.1				
COPPIA DI PICCO *Peak torque*	Cp	Nm	7.5	7.5					7.5	7.5				
CORRENTE DI PICCO *Peak current*	Ip	A	12.6	37.2					18	60.6				
RENDIMENTO *Efficiency*	-	%	77	77					80	80				
DATI MECCANICI *Mechanical data*														
INERZIA ROTORE *Rotor inertia*	J	Kg/m²	0.00113	0.00113					0.00113	0.00113				
MAX. ACCELLERAZ. TEORICA *Max theorical accelleration*	a	rad/ sec²	6640	6640					6640	6640				
CARICO ASSIALE MAX. *Max axial load*	Fa	N	119	119					119	119				
CARICO RADIALE MASSIMO *Max radial load*	Fr	N	480	480					480	480				
GRADO DI PROTEZIONE *Protection (IEC.34.5)*	-	IP	54	54					54	54				
PESO *Weight*	-	Kg	7.5	7.5					7.5	7.5				
DATI ELETTRICI *Winding data*														
COSTANTE DI TEMPO TERMICA *Thermal time constant*	Tt	min	90	90					90	90				
COSTANTE DI TEMPO ELETTRICA *Electrical time constant*	Te	ms	6.3	5					6	2.4				
RESISTENZA D'ARMATURA *Armature resistance*	Rm	Ohm	7.5	0.93					3.9	0.33				
INDUTTANZA D'ARMATURA *Armature inductance*	La	mH	47	4.7					23.4	0.8				
CLASSE ISOLAMENTO *Insulation class*	-	-	F	F					F	F				
FATTORE DI SERVIZIO *Duty*	-	-	S1	S1					S1	S1				
FATTORE DI FORMA *Form factor*	-	-	1	1					1	1				
TEMPERATURA AMBIENTE *Ambient temperature*	-	C°	25	25					25	25				
ALTEZZA *Height*	-	m	1000	1000					1000	1000				
TOLLERANZE *Tolerance*	-	%	+/-5	+/-5					+/-5	+/-5				

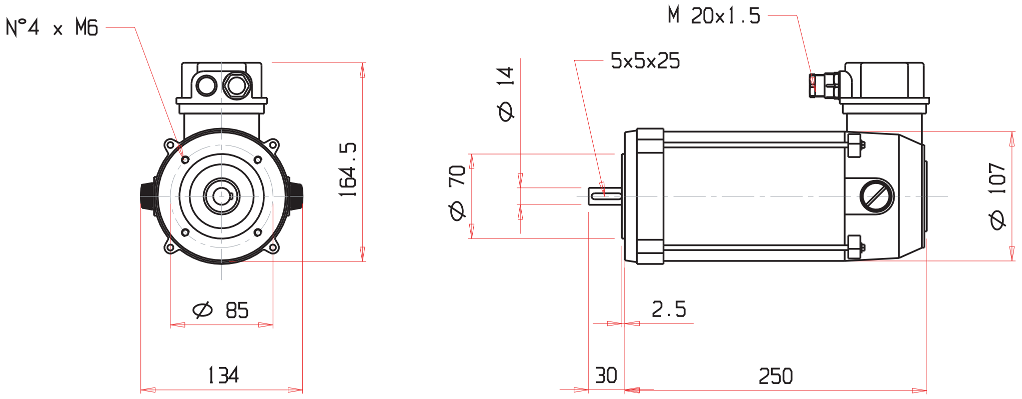
** Tensioni non a catalogo a richiesta
Not depliant voltage to request

SERIE
Series

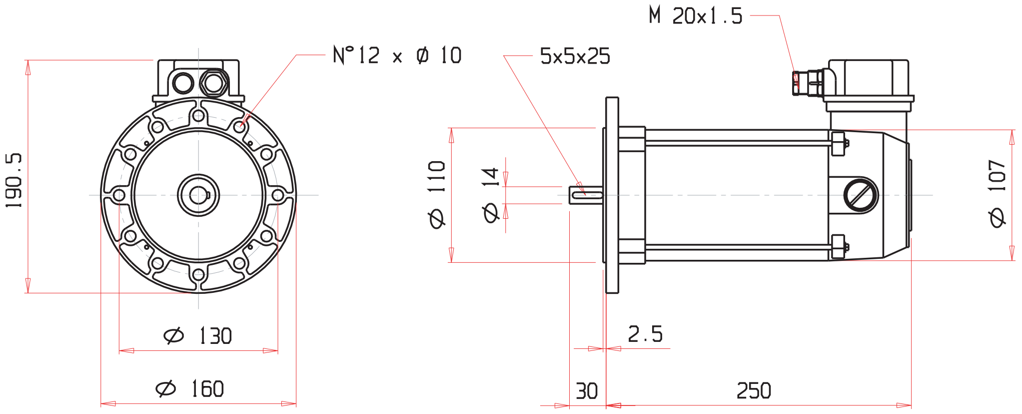
R3M

DIMENSIONI *Dimensions*

B14 M71



B5 M71



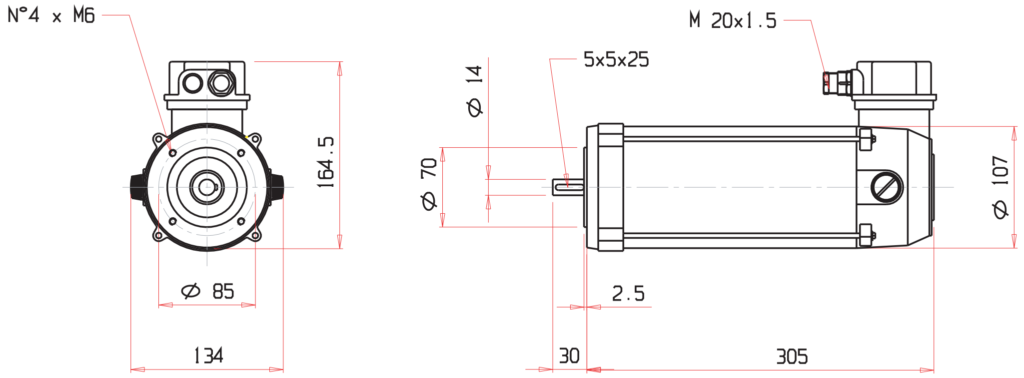
DATI MOTORE ***Motor ratings***	**SIMBOLI** ***Symbols***	**UNITÀ** ***Units***	**SERIE** ***Series*** **R3L**											
COPPIA ALLA VELOCITÀ NOMINALE *Torque at rated speed*	Cn	Nm	1.9	1.9					1.9	1.9				
VELOCITÀ NOMINALE *Rated speed*	Nm	RPM	2000	2000					3000	3000				
POTENZA NOMINALE *Reated output*	Pu	W	400	400					600	600				
TENSIONE NOMINALE *Rated Voltage*	Vn	V	170	48					170	48				
CORRENTE NOMINALE *Rated Current*	In	A	2.9	10.1					4.5	15.4				
COPPIA DI PICCO *Peak torque*	Cp	Nm	11.4	11.4					11.4	11.4				
CORRENTE DI PICCO *Peak current*	Ip	A	17.4	60.6					27.6	92.4				
RENDIMENTO *Efficiency*	-	%	83	80					80	80				
DATI MECCANICI *Mechanical data*														
INERZIA ROTORE *Rotor inertia*	J	Kg/m²	0.00169	0.00169					0.00169	0.00169				
MAX. ACCELLERAZ. TEORICA *Max theorical accelleration*	a	rad/ sec²	6750	6750					6750	6750				
CARICO ASSIALE MAX. *Max axial load*	Fa	N	119	119					119	119				
CARICO RADIALE MASSIMO *Max radial load*	Fr	N	480	480					480	480				
GRADO DI PROTEZIONE *Protection (IEC.34.5)*	-	IP	54	54					54	54				
PESO *Weight*	-	Kg	10.3	10.3					10.3	10.3				
DATI ELETTRICI *Winding data*														
COSTANTE DI TEMPO TERMICA *Thermal time constant*	Tt	min	90	90					90	90				
COSTANTE DI TEMPO ELETTRICA *Electrical time constant*	Te	ms	7	8					7	5.5				
RESISTENZA D'ARMATURA *Armature resistance*	Rm	Ohm	4.9	0.36					2.5	0.2				
INDUTTANZA D'ARMATURA *Armature inductance*	La	mH	34.5	2.9					17.5	1.1				
CLASSE ISOLAMENTO *Insulation class*	-	-	F	F					F	F				
FATTORE DI SERVIZIO *Duty*	-	-	S1	S1					S1	S1				
FATTORE DI FORMA *Form factor*	-	-	1	1					1	1				
TEMPERATURA AMBIENTE *Ambient temperature*	-	C°	25	25					25	25				
ALTEZZA *Height*	-	m	1000	1000					1000	1000				
TOLLERANZE *Tolerance*	-	%	+/-5	+/-5					+/-5	+/-5				

** Tensioni non a catalogo a richiesta
Not depliant voltage to request

SERIE *Series* **R3L**

DIMENSIONI *Dimensions*

B14 M71



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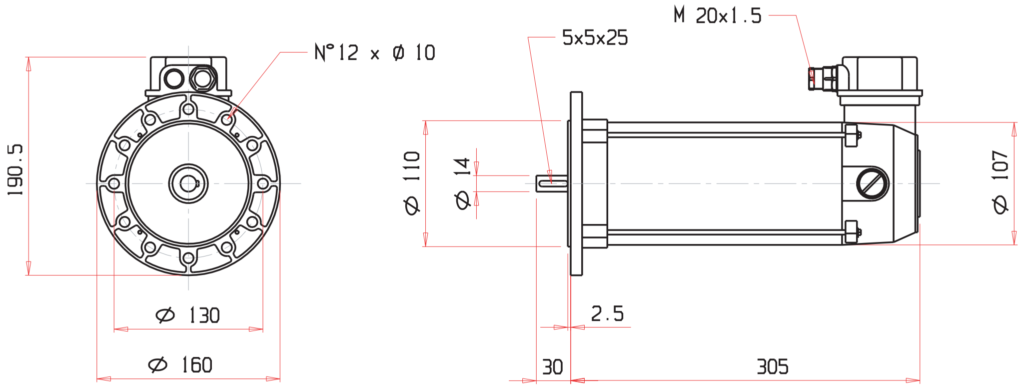
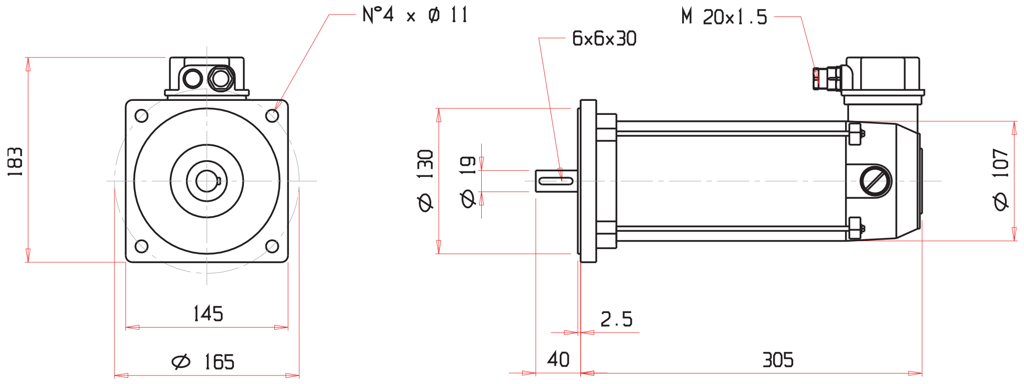


B5 M80



OPZIONI ***Optional***	**SIMBOLI** ***Symbols***	**UNITÀ** ***Units***	**SERIE** ***Series*** **R3**						
TIPO MOTORE *Motor type*	-	-	R3S	R3M	R3L				
DATI DINAMO TACHIMETRICA 4 POLI *4 Poles tacho generator data*									
COSTANTE DI TENSIONE *Voltage constant*	En	V/KRPM	10	10	10				
ONDULAZIONE DI PICCO *Ripple*	dEc	%	0,5	0,5	0,5				
LINEARITÀ A 6000 RPM *Linearity at 6000 RPM*	dE	%	0,15	0,15	0,15				
ERRORE DI REVERSIBILITÀ *Reversibility error*	dEo	%	0,5	0,5	0,5				
RESISTENZA *Resistance*	Ra	Ohm	112	112	112				
N° POLI *N° poles*	-	-	4	4	4				
LUNGHEZZA MOTORE + D.T *Motor lenght + T.G*	L1	mm	222	282	337				
DATI DINAMO TACHIMETRICA RE10E *RE10E tacho generator data*									
COSTANTE DI TENSIONE *Voltage constant*	En	V/KRPM	10	10	10				
ONDULAZIONE DI PICCO *Ripple*	dEc	%	1,6	1,6	1,6				
LINEARITÀ A 6000 RPM *Linearity at 6000 RPM*	dE	%	0,5	0,5	0,5				
ERRORE DI REVERSIBILITÀ *Reversibility error*	dEo	%	0,5	0,5	0,5				
RESISTENZA *Resistance*	Ra	Ohm	112	112	112				
N° POLI *N° poles*	-	-	4	4	4				
LUNGHEZZA MOTORE + D.T *Motor lenght + T.G*	L2	mm	222	282	337				
DATI ALTERNATORE *Alternator data*									
COSTANTE DI TENSIONE *Voltage constant*	En	V/KRPM	24	24	24				
MAX VELOCITÀ *Max speed*	Nmax	RPM	10000	10000	10000				
CORRENTE NOMINALE *Rated current*	In	mA	5	5	5				
CORRENTE MASSIMA *Max current*	Imax	mA	100	100	100				
LUNGHEZZA MOTORE + A.T *Motor lenght + alternator*	L3	mm	226	286	341				
DATI FRENO DI STAZIONAMENTO *Parking brake data*									
COPPIA STATICA *Static torque*	C	Nm	4,5	4,5	4,5				
TENSIONE DI ALIMENTAZIONE *Power supply voltage*	E	Vdc	24	24	24				
CORRENTE *Current*	I	A	0,95	0,95	0,95				
POTENZA ASSORBITA *Input power*	Pa	W	23	23	23				
LUNGHEZZA MOTORE + FRENO *Motor lenght + brake*	L4	mm	227	287	342				

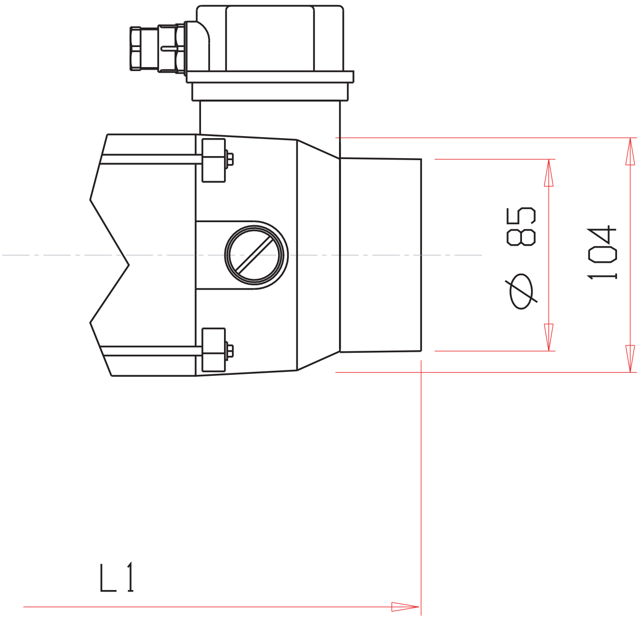
TOLLERANZE *Tolerance*	-	%	-/+ 5	-/+ 5	-/+ 5				
TEMPERATURA AMBIENTE *Ambient temperature*	-	°C	25	25	25				

OPZIONI SERIE
Options serie

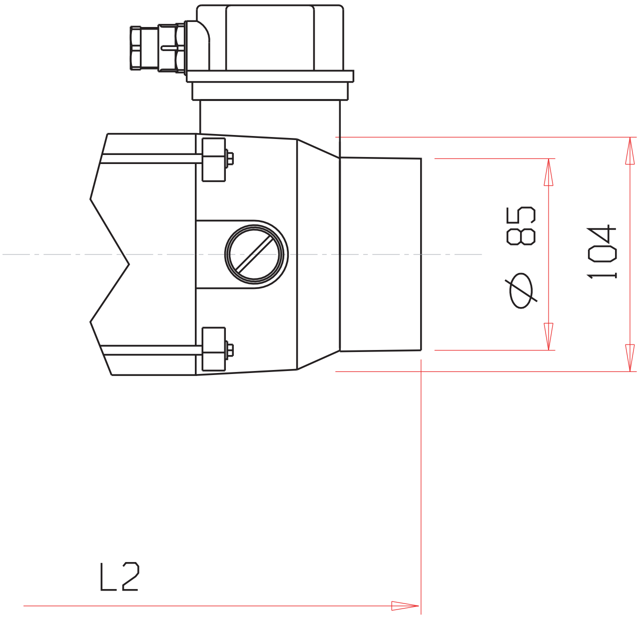
R3

DIMENSIONI *Dimensions*

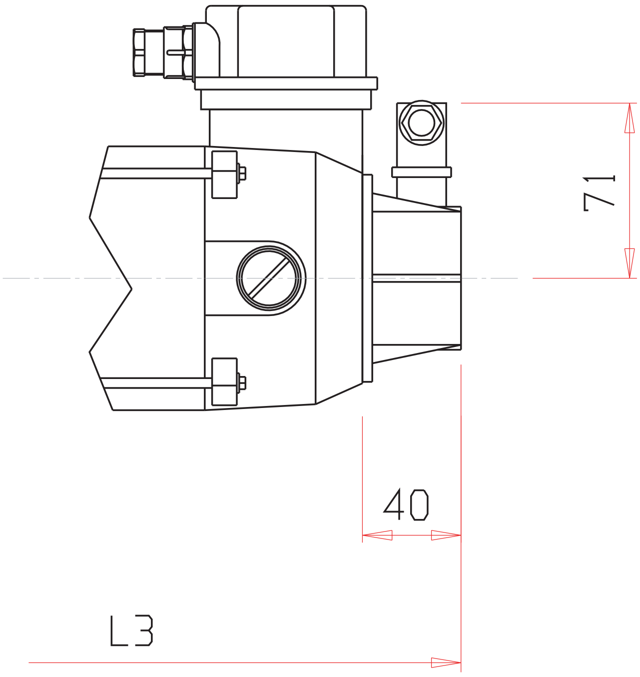
DINAMO TACHIMETRICA 4 POLI
Tacho generators 4 poles



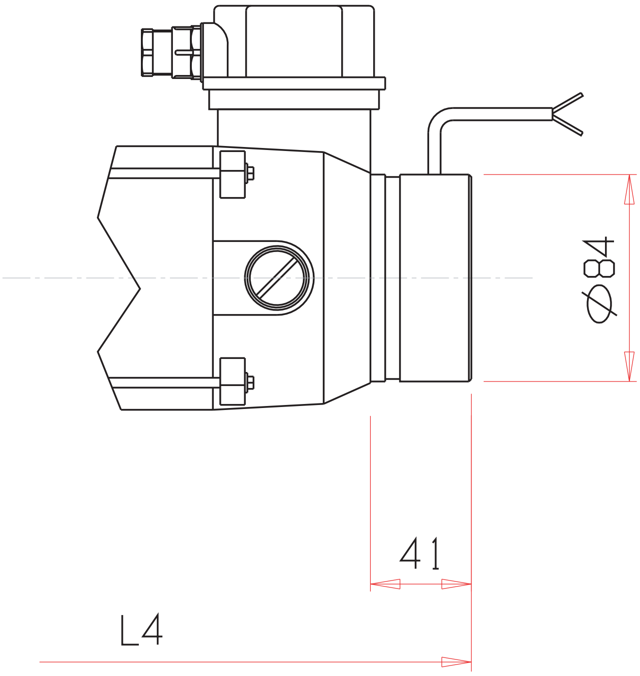
DINAMO TACHIMETRICA RE10E
RE10E Tacho generators



ALTERNATORE
Alternator



FRENO DI STAZIONAMENTO
Parking brake



Dati indicativi non impegnativi con riserva di modifica
Specification are indicatives not bindings with subject to modification

SIEMENS

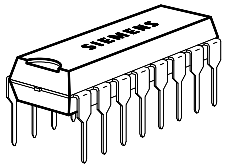
Phase Control IC

TCA 785

Bipolar IC

Features

- Reliable recognition of zero passage
- Large application scope
- May be used as zero point switch
- LSL compatible
- Three-phase operation possible (3 ICs)
- Output current 250 mA
- Large ramp current range
- Wide temperature range

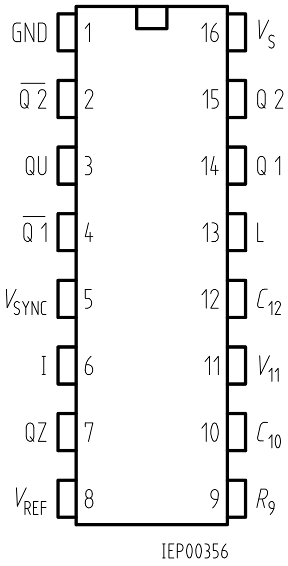


P-DIP-16-1

Type	Ordering Code	Package
TCA 785	Q67000-A2321	P-DIP-16-1

This phase control IC is intended to control thyristors, triacs, and transistors. The trigger pulses can be shifted within a phase angle between 0 ° and 180 °. Typical applications include converter circuits, AC controllers and three-phase current controllers.

This IC replaces the previous types TCA 780 and TCA 780 D.



Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground
2 3 4	$\overline{\text{Q2}}$ Q U $\overline{\text{Q2}}$	Output 2 inverted Output U Output 1 inverted
5	V_{SYNC}	Synchronous voltage
6 7	I Q Z	Inhibit Output Z
8	V_{REF}	Stabilized voltage
9 10	R_9 C_{10}	Ramp resistance Ramp capacitance
11	V_{11}	Control voltage
12	C_{12}	Pulse extension
13	L	Long pulse
14 15	Q 1 Q 2	Output 1 Output 2
16	V_S	Supply voltage

Functional Description

The synchronization signal is obtained via a high-ohmic resistance from the line voltage (voltage V_5). A zero voltage detector evaluates the zero passages and transfers them to the synchronization register.

This synchronization register controls a ramp generator, the capacitor C_{10} of which is charged by a constant current (determined by R_9). If the ramp voltage V_{10} exceeds the control voltage V_{11} (triggering angle φ), a signal is processed to the logic. Dependent on the magnitude of the control voltage V_{11}, the triggering angle φ can be shifted within a phase angle of 0° to 180°.

For every half wave, a positive pulse of approx. 30 µs duration appears at the outputs Q 1 and Q 2. The pulse duration can be prolonged up to 180° via a capacitor C_{12}. If pin 12 is connected to ground, pulses with a duration between φ and 180° will result.

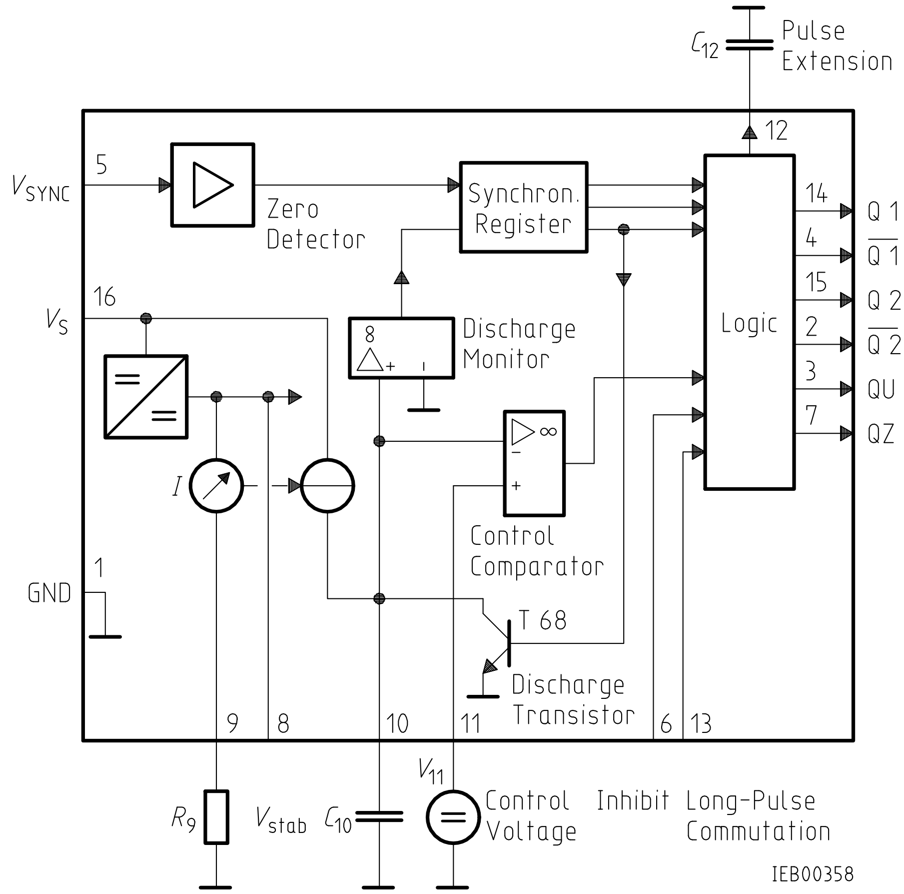
Outputs $\overline{Q1}$ and $\overline{Q2}$ supply the inverse signals of Q 1 and Q 2.

A signal of φ +180° which can be used for controlling an external logic,is available at pin 3.

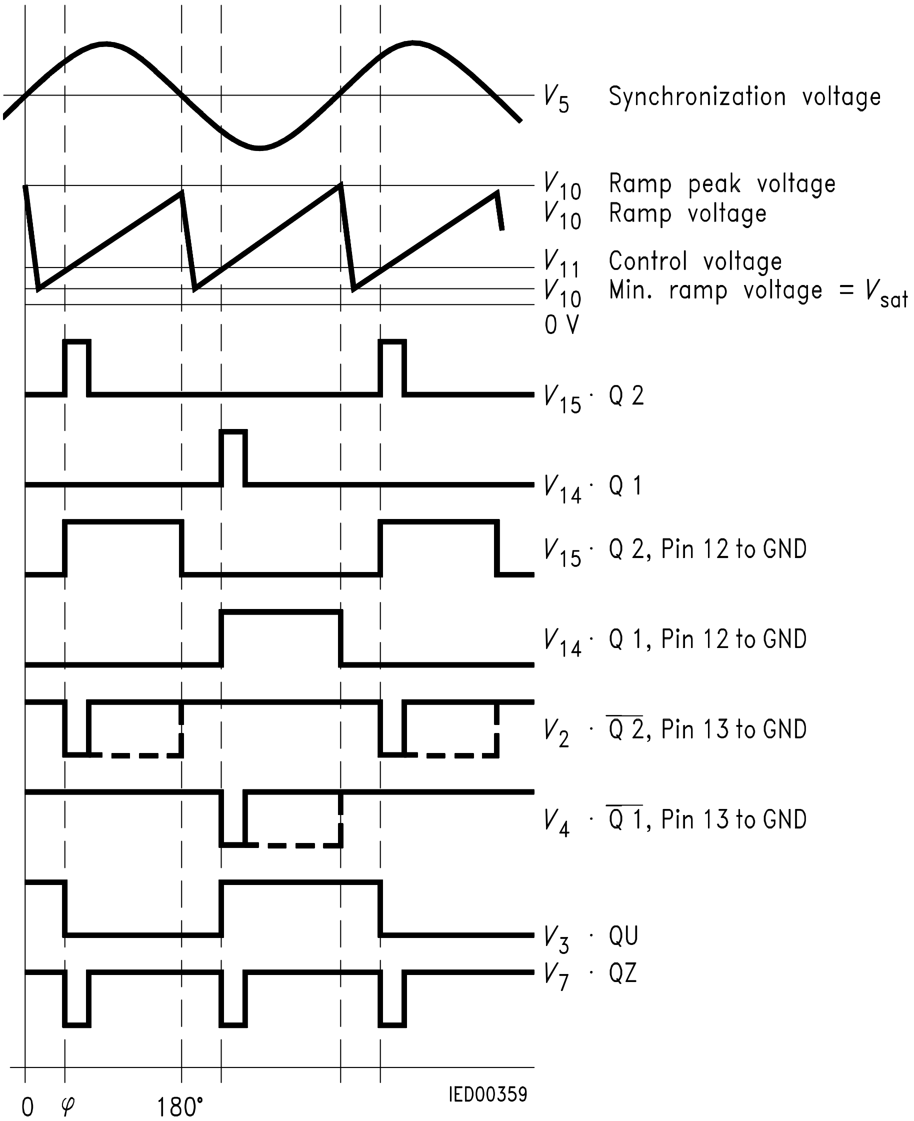
A signal which corresponds to the NOR link of Q 1 and Q 2 is available at output Q Z (pin 7).

The inhibit input can be used to disable outputs Q1, Q2 and $\overline{Q1}$, $\overline{Q2}$.

Pin 13 can be used to extend the outputs $\overline{Q1}$ and $\overline{Q2}$ to full pulse length (180° – φ).



Block Diagram



Pulse Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	– 0.5	18	V
Output current at pin 14, 15	I_Q	– 10	400	mA
Inhibit voltage Control voltage Voltage short-pulse circuit	V_6 V_{11} V_{13}	– 0.5 – 0.5 – 0.5	V_S V_S V_S	V V V
Synchronization input current	V_5	– 200	± 200	μA
Output voltage at pin 14, 15	V_Q		V_S	V
Output current at pin 2, 3, 4, 7	I_Q		10	mA
Output voltage at pin 2, 3, 4, 7	V_Q		V_S	V
Junction temperature Storage temperature	T_j T_{stg}	 – 55	150 125	˚C ˚C
Thermal resistance system - air	$R_{th\ SA}$		80	K/W

Operating Range

Supply voltage	V_S	8	18	V
Operating frequency	f	10	500	Hz
Ambient temperature	T_A	– 25	85	˚C

Characteristics

$8 \leq V_S \leq 18$ V; -25 ˚C $\leq T_A \leq 85$ ˚C; $f = 50$ Hz

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Supply current consumption S1 … S6 open $V_{11} = 0$ V $C_{10} = 47$ nF; $R_9 = 100$ kΩ	I_S	4.5	6.5	10	mA	1
Synchronization pin 5 Input current R_2 varied Offset voltage	 $I_{5\ rms}$ ΔV_5	 30 	 30	 200 75	 μA mV	 1 4
Control input pin 11 Control voltage range Input resistance	 V_{11} R_{11}	 0.2 	 15	 $V_{10\ peak}$ 	 V kΩ	 1 5

Characteristics (cont’d)
$8 \leq V_S \leq 18$ V; – 25 ˚C ≤ $T_A \leq 85$ ˚C; $f = 50$ Hz

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Ramp generator						
Charge current	I_{10}	10		1000	µA	
Max. ramp voltage	V_{10}			$V_2 - 2$	V	1
Saturation voltage at capacitor	V_{10}	100	225	350	mV	1.6
Ramp resistance	R_9	3		300	kΩ	1
Sawtooth return time	t_f		80		µs	1
Inhibit pin 6 switch-over of pin 7						
Outputs disabled	$V_{6\,L}$		3.3	2.5	V	1
Outputs enabled	$V_{6\,H}$	4	3.3		V	1
Signal transition time	t_r	1		5	µs	1
Input current $V_6 = 8$ V	$I_{6\,H}$		500	800	µA	1
Input current $V_6 = 1.7$ V	$-I_{6\,L}$	80	150	200	µA	1
Deviation of I_{10} R_9 = const. $V_S = 12$ V; $C_{10} = 47$ nF	I_{10}	– 5		5	%	1
Deviation of I_{10} R_9 = const. $V_S = 8$ V to 18 V	I_{10}	– 20		20	%	1
Deviation of the ramp voltage between 2 following half-waves, V_S = const.	$\Delta V_{10\,max}$		± 1		%	
Long pulse switch-over pin 13 switch-over of S8						
Short pulse at output	$V_{13\,H}$	3.5	2.5		V	1
Long pulse at output	$V_{13\,L}$		2.5	2	V	1
Input current $V_{13} = 8$ V	$I_{13\,H}$			10	µA	1
Input current $V_{13} = 1.7$ V	$-I_{13\,L}$	45	65	100	µA	1
Outputs pin 2, 3, 4, 7						
Reverse current $V_Q = V_S$	I_{CEO}			10	µA	2.6
Saturation voltage $I_Q = 2$ mA	V_{sat}	0.1	0.4	2	V	2.6

Characteristics (cont'd)
$8 \leq V_S \leq 18$ V; – 25 ˚C ≤ $T_A \leq 85$ ˚C; $f = 50$ Hz

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Outputs pin 14, 15						
H-output voltage $-I_Q = 250$ mA	$V_{14/15\,H}$	$V_S - 3$	$V_S - 2.5$	$V_S - 1.0$	V	3.6
L-output voltage $I_Q = 2$ mA	$V_{14/15\,L}$	0.3	0.8	2	V	2.6
Pulse width (short pulse) S9 open	t_p	20	30	40	µs	1
Pulse width (short pulse) with C_{12}	t_p	530	620	760	µs/ nF	1
Internal voltage control						
Reference voltage Parallel connection of 10 ICs possible	V_{REF}	2.8	3.1	3.4	V	1
TC of reference voltage	α_{REF}		2×10^{-4}	5×10^{-4}	1/K	1

Application Hints for External Components

		min	max	
Ramp capacitance	C_{10}	500 pF	1 µF[1]	The minimum and maximum values of I_{10} are to be observed

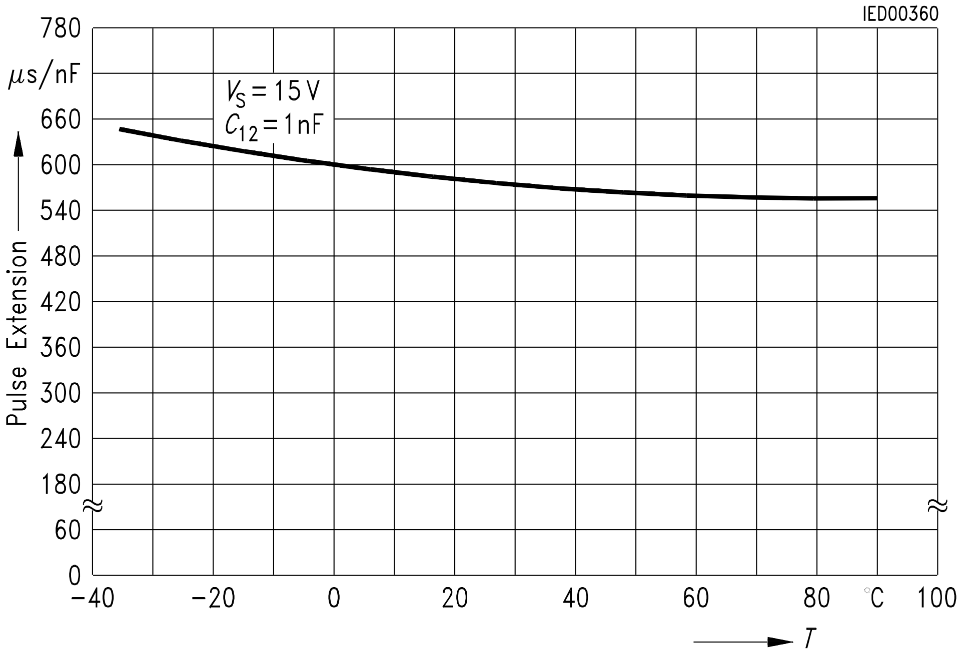
Triggering point $t_{Tr} = \frac{V_{11} \times R_9 \times C_{10}}{V_{REF} \times K}$ [2]

Charge current $I_{10} = \frac{V_{REF} \times K}{R_9}$ [2]

Ramp voltage

$V_{10\,max} = V_S - 2\,V$ $V_{10} = \frac{V_{REF} \times K \times t}{R_9 \times C_{10}}$ [2]

Pulse Extension versus Temperature



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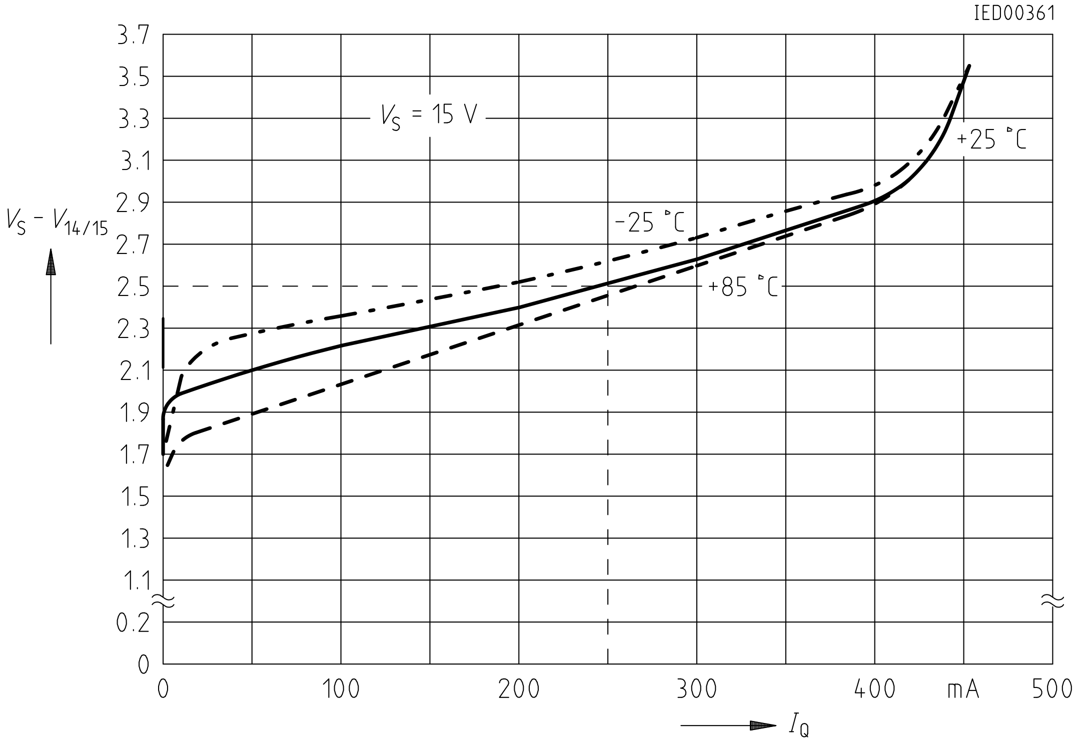
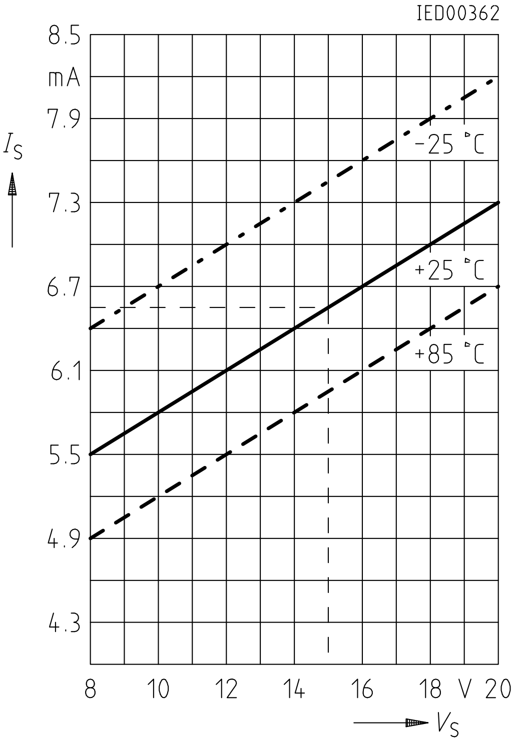
[1] Attention to flyback times

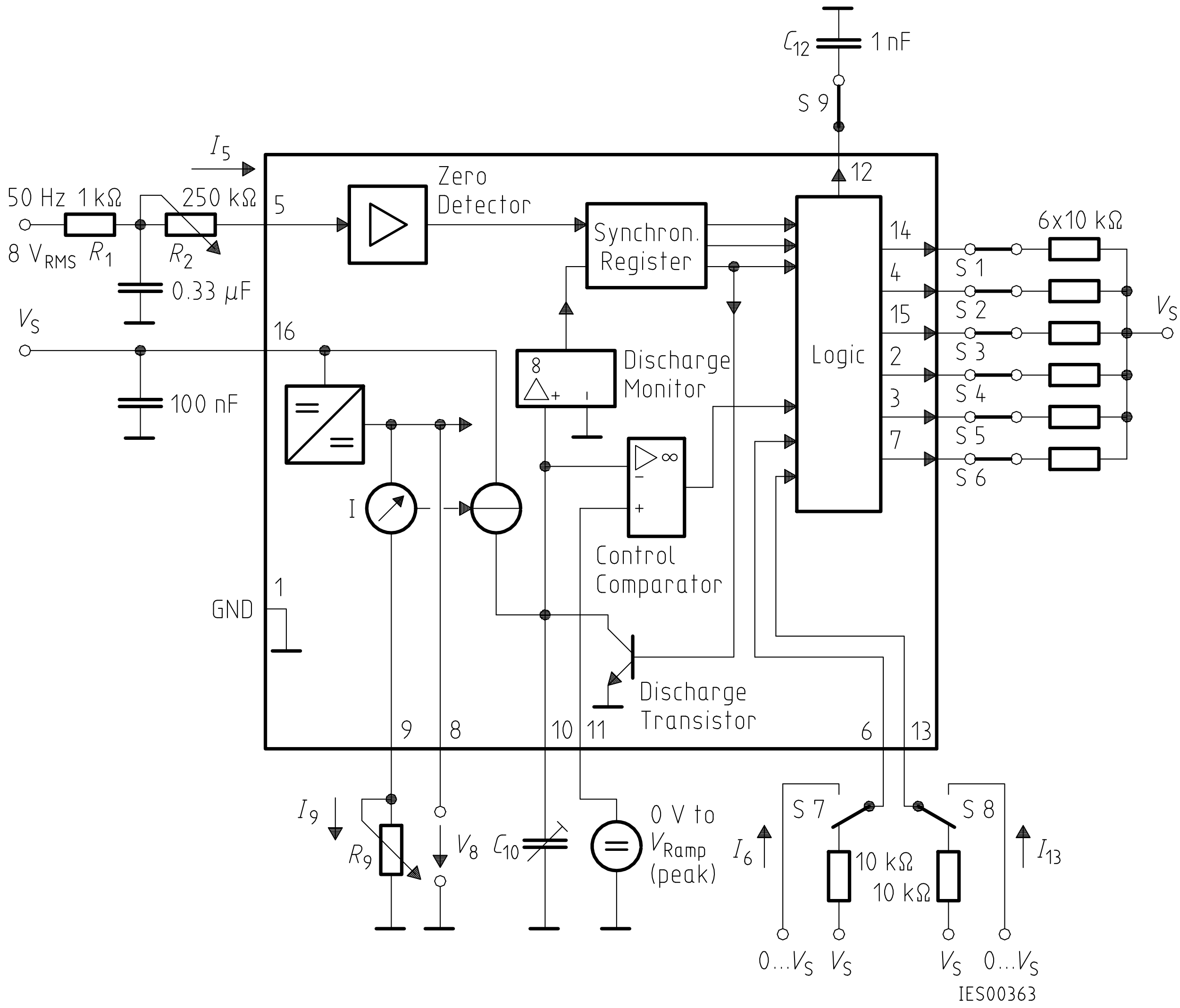
[2] $K = 1.10 \pm 20\ \%$

Output Voltage measured to + V_S



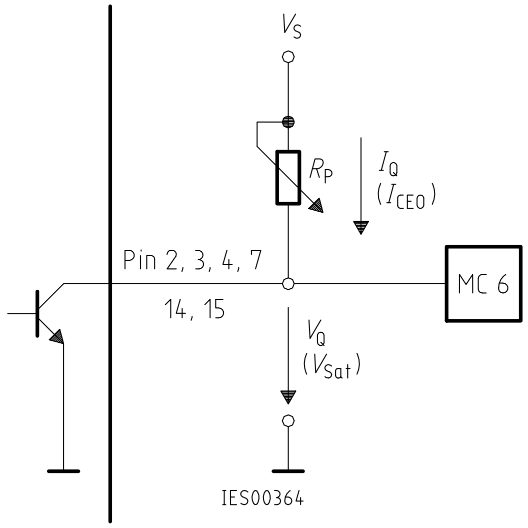
Supply Current versus Supply Voltage





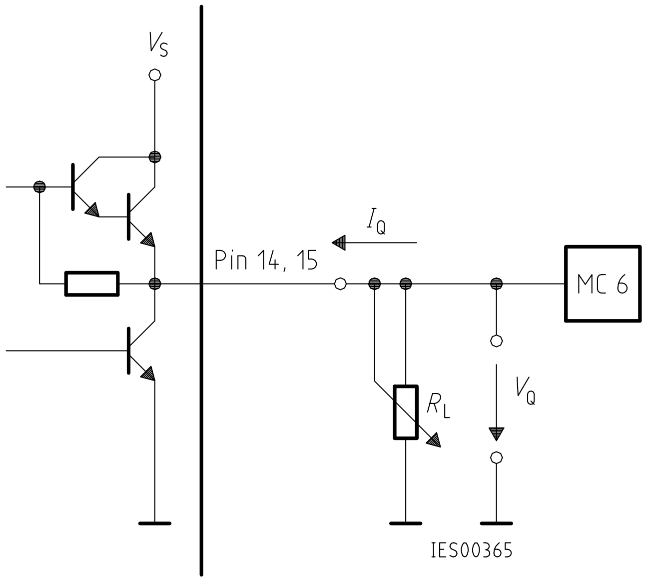
It is necessary for all measurements to adjust the ramp with the aid of C_{10} and R_9 in the way that $3\,V \leq V_{ramp\,max} \leq V_S - 2\,V$ e.g. C_{10} = 47 nF; 18 V: R_9 = 47 kΩ; 8 V: R_9 = 120 kΩ

Test Circuit 1



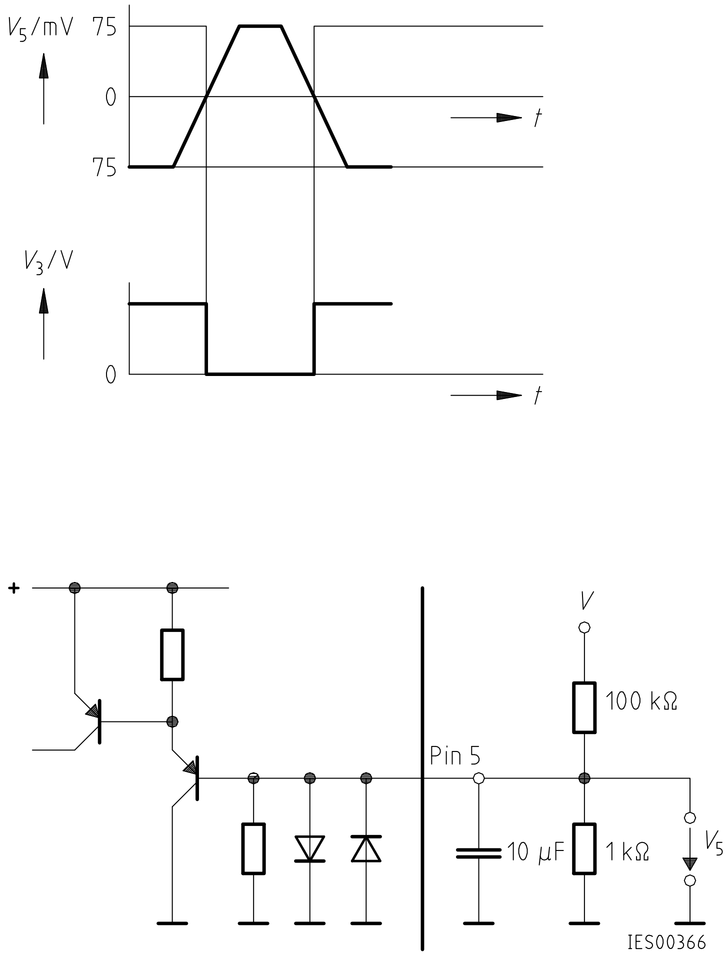
The remaining pins are connected as in test circuit 1

Test Circuit 2



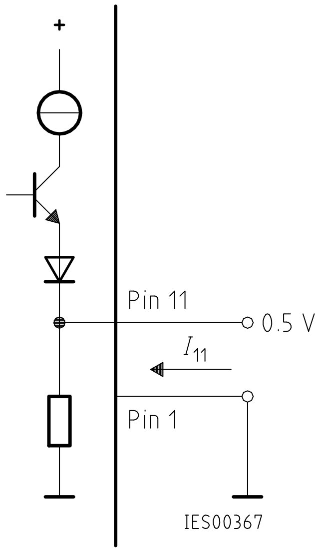
The remaining pins are connected as in test circuit 1

Test Circuit 3

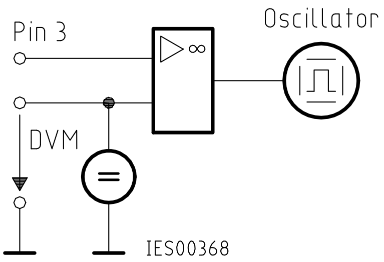


Remaining pins are connected as in test circuit 1
The 10 µF capacitor at pin 5 serves only for test purposes

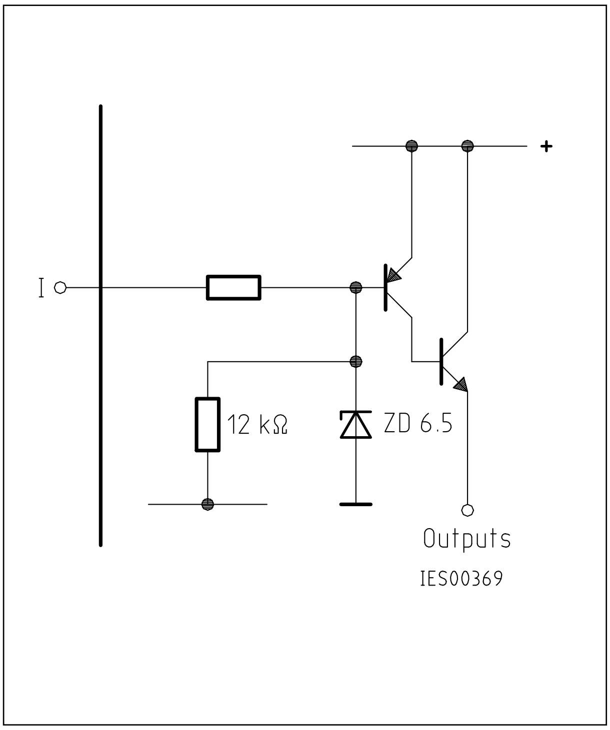
Test Circuit 4



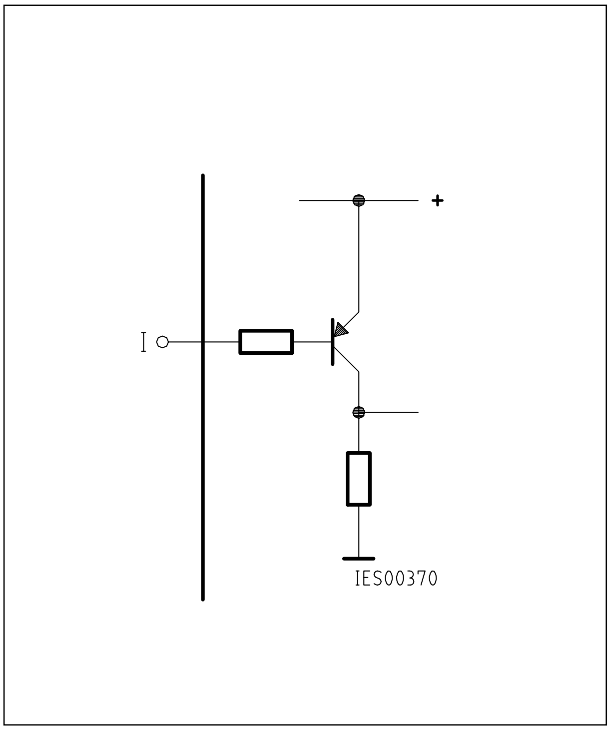
Test Circuit 5



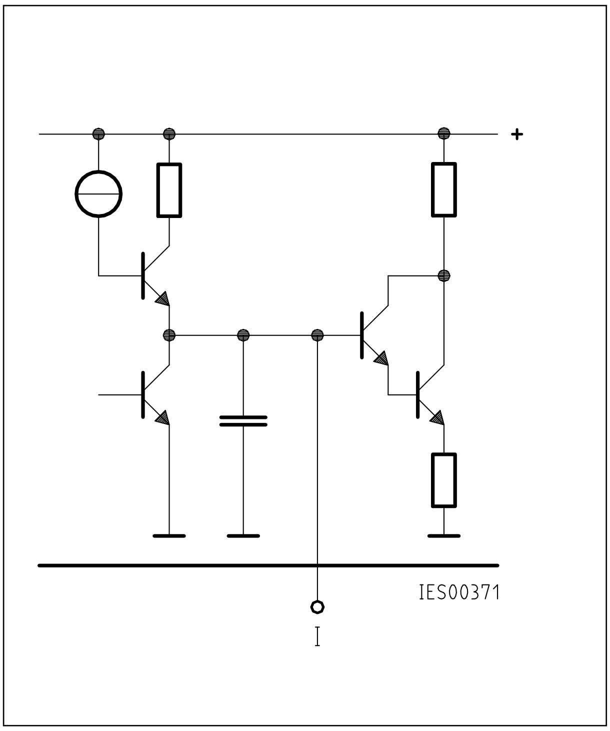
Test Circuit 6



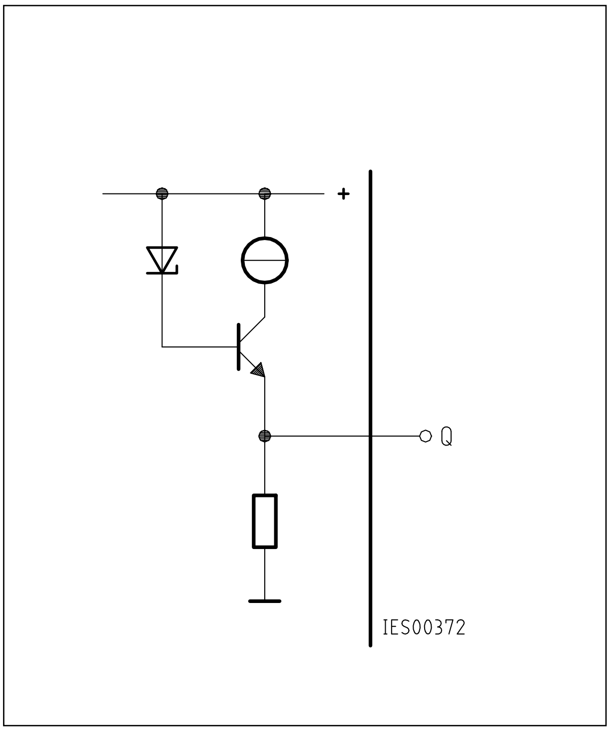
Inhibit 6



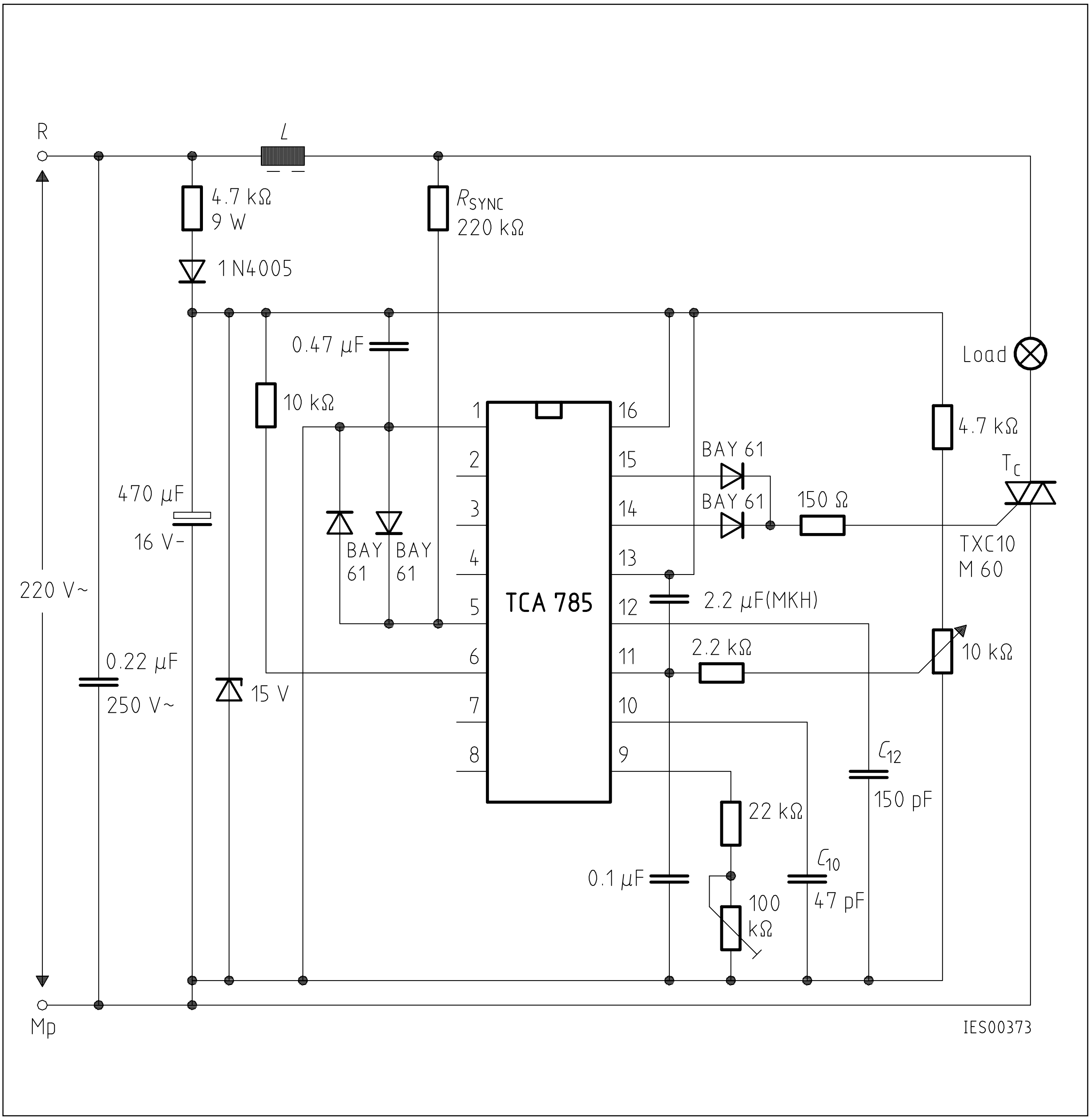
Long Pulse 13



Pulse Extension 12

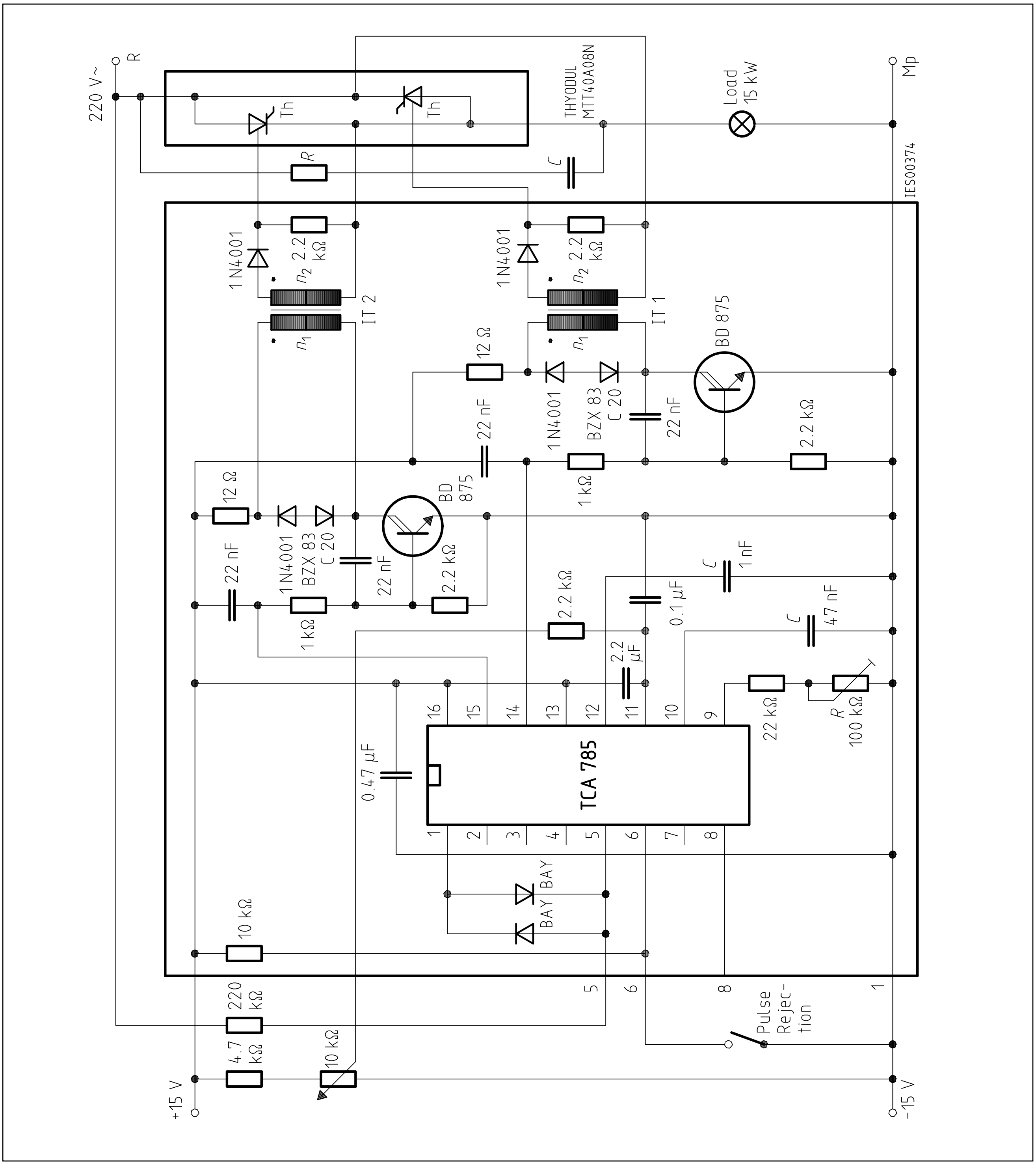


Reference Voltage 8



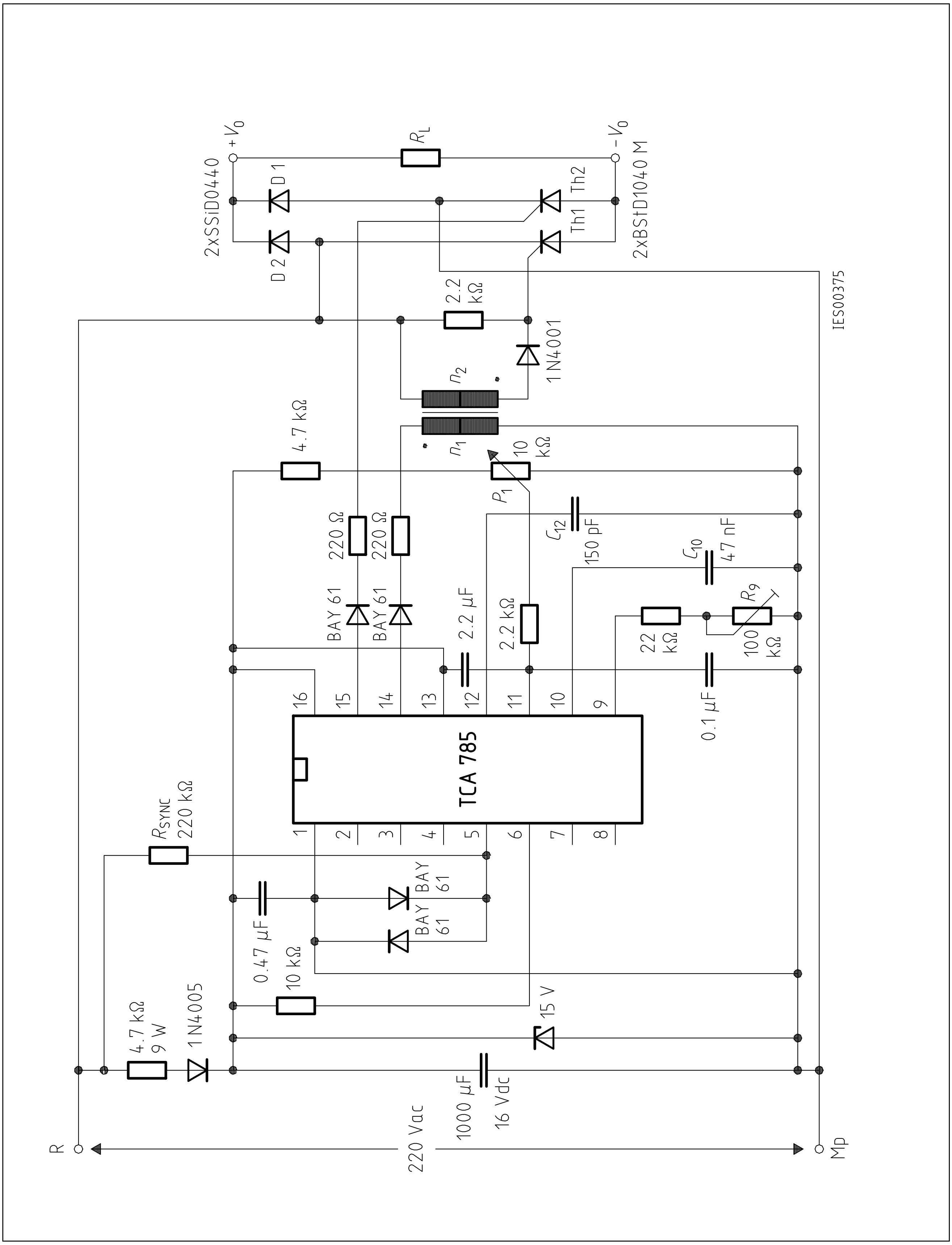
Application Examples
Triac Control for up to 50 mA Gate Trigger Current

A phase control with a directly controlled triac is shown in the figure. The triggering angle of the triac can be adjusted continuously between 0° and 180° with the aid of an external potentiometer. During the positive half-wave of the line voltage, the triac receives a positive gate pulse from the IC output pin 15. During the negative half-wave, it also receives a positive trigger pulse from pin 14. The trigger pulse width is approx. 100 µs.

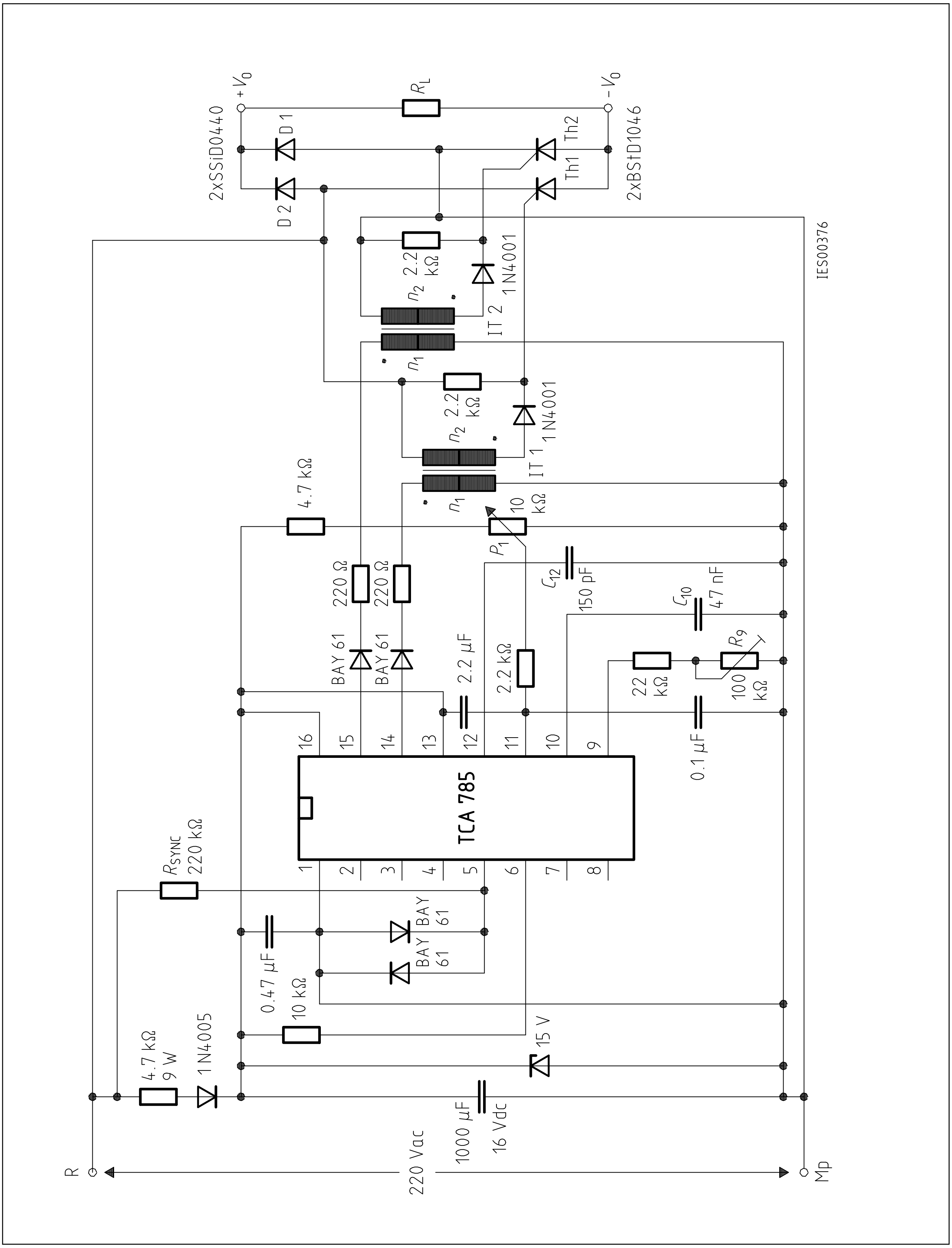


Fully Controlled AC Power Controller
Circuit for Two High-Power Thyristors

Shown is the possibility to trigger two antiparalleled thyristors with one IC TCA 785. The trigger pulse can be shifted continuously within a phase angle between 0˚ and 180˚ by means of a potentiometer. During the negative line half-wave the trigger pulse of pin 14 is fed to the relevant thyristor via a trigger pulse transformer. During the positive line half-wave, the gate of the second thyristor is triggered by a trigger pulse transformer at pin 15.



Half-Controlled Single-Phase Bridge Circuit with Trigger Pulse Transformer and Direct Control for Low-Power Thyristors



Half-Controlled Single-Phase Bridge Circuit with Two Trigger Pulse Transformers for Low-Power Thyristors

GENERAL DESCRIPTION

Passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

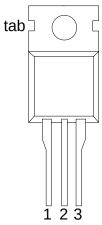
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT151-	**500R**	**650R**	**800R**	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	500	650	800	V
$I_{T(AV)}$	Average on-state current	7.5	7.5	7.5	A
$I_{T(RMS)}$	RMS on-state current	12	12	12	A
I_{TSM}	Non-repetitive peak on-state current	100	100	100	A

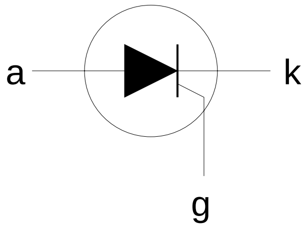
PINNING - TO220AB

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500R	**-650R**	**-800R**	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	500[1]	650[1]	800	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{mb} \leq 109$ ˚C	-	7.5			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	12			A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 25$ ˚C prior to surge					
		t = 10 ms	-	100			A
		t = 8.3 ms	-	110			A
I^2t	I^2t for fusing	t = 10 ms	-	50			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 50$ mA; $dI_G/dt = 50$ mA/µs	-	50			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
V_{RGM}	Peak reverse gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

---

[1] Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	-	1.3	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A	-	2	15	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A	-	10	40	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	7	20	mA
V_T	On-state voltage	I_T = 23 A	-	1.4	1.75	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.6	1.5	V
		$V_D = V_{DRM(max)}$; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform;				
		Gate open circuit	50	130	-	V/µs
		R_{GK} = 100 Ω	200	1000	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 40 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 20 A; V_R = 25 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 50 V/µs; R_{GK} = 100 Ω	-	70	-	µs

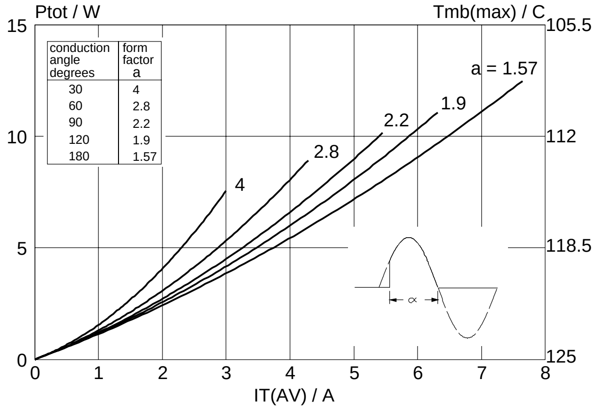


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.

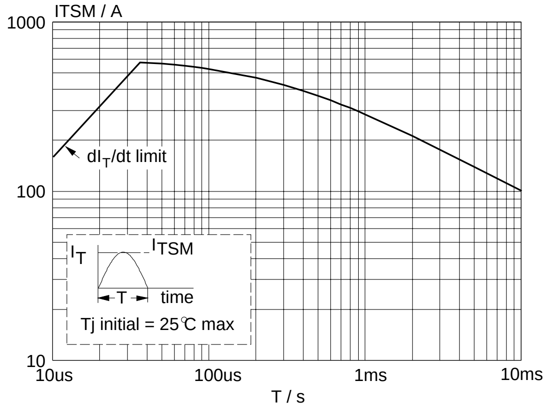


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 10ms.

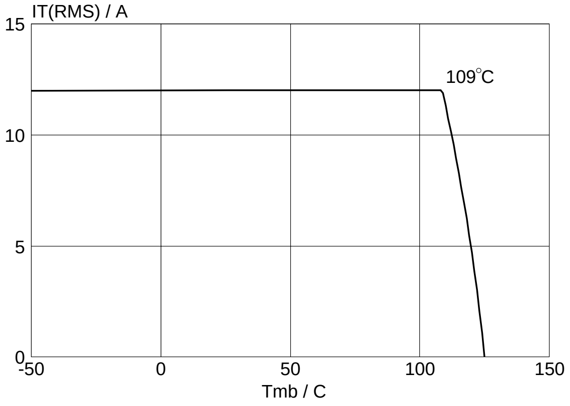


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

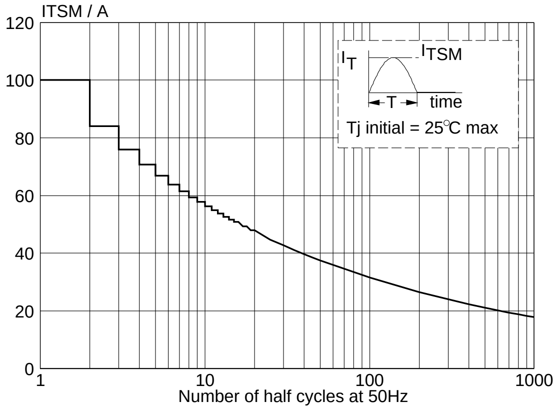


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

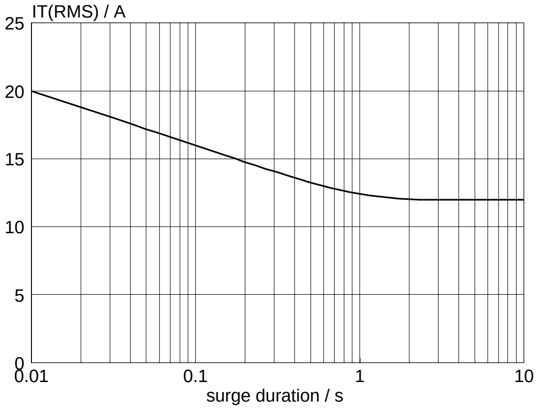


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 109^\circ C$.

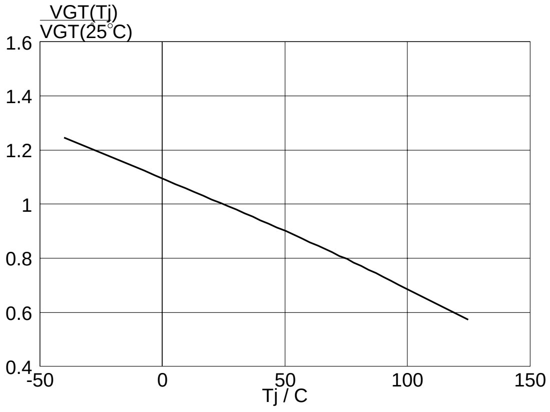


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ $V_{GT}(25^\circ C)$, versus junction temperature T_j.

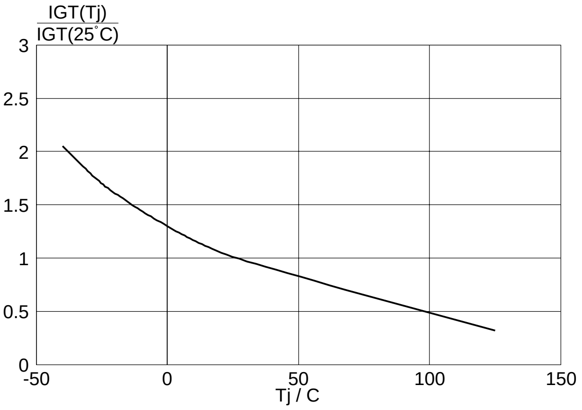


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

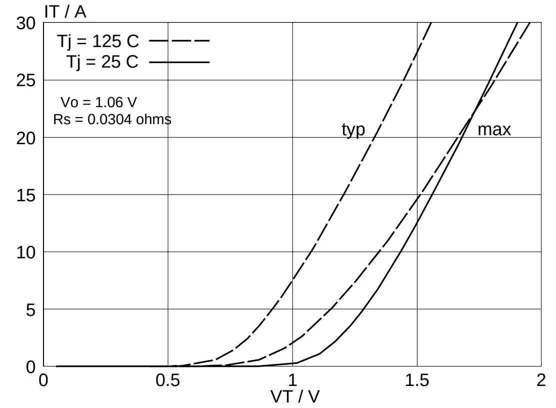


Fig.10. Typical and maximum on-state characteristic.

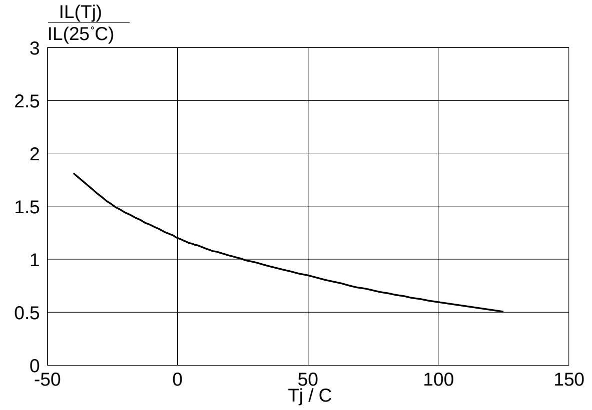


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

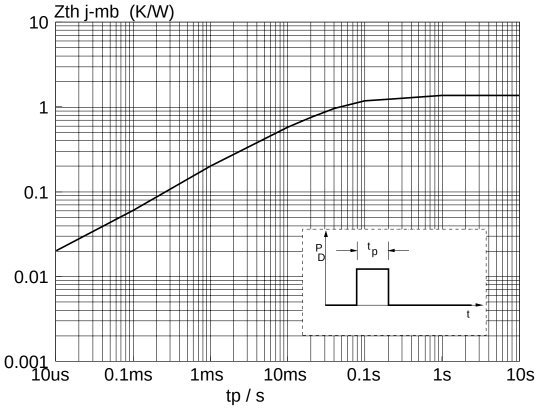


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

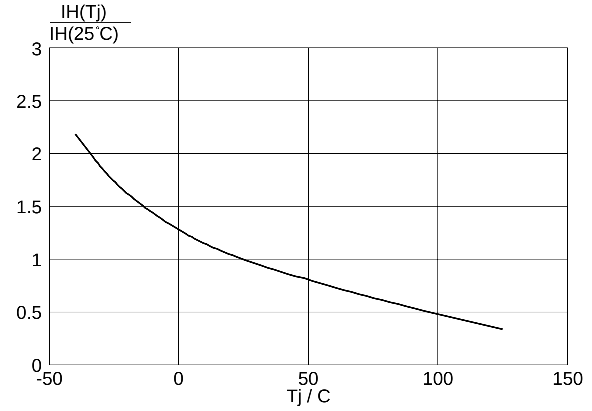


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

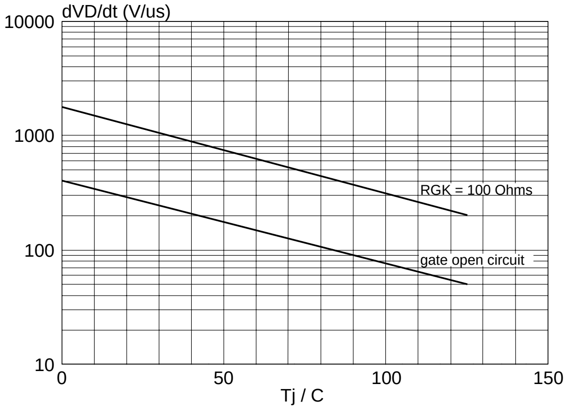


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

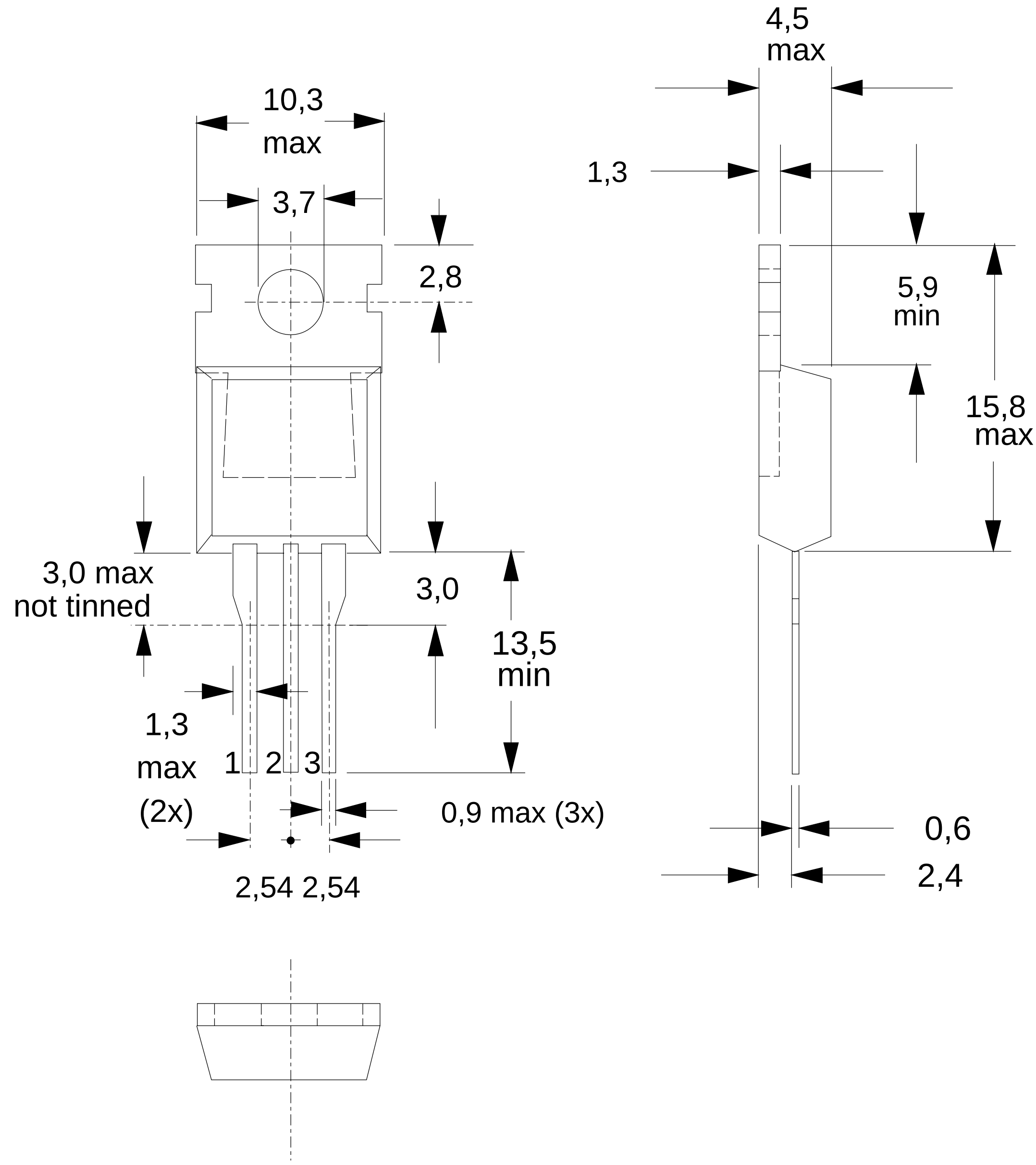


Fig.13. SOT78 (TO220AB). pin 2 connected to mounting base.

Notes
1. Refer to mounting instructions for SOT78 (TO220) envelopes.
2. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

FS28-1300-C2

Description:

The FS28-1300-C2 is a series/parallel primary and dual secondary, split bobbin design which operates with either a parallel input of 115V or a series input of 230V. The secondaries are 14V @ 1.3A each. They can be used independently (up to 300V difference between them) or in series for double the voltage or in parallel for double the current. The split bobbin design eliminates the need for costly electrostatic shielding.

Electrical Specifications (@25C)

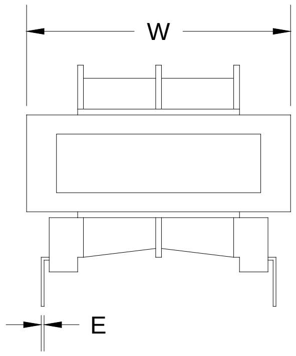
1. Maximum Power: 36.0VA
2. Primary: Series: 230V; Parallel: 115V
3. Secondaries: 14.0V @ 1.3A each
4. Voltage Regulation: 25% TYP @ full load to no load
5. Temperature Rise: 25C TYP
6. Hipot tested 100% at 4200 VRMS pri to sec
7. Hipot tested 100% at 2160 VRMS sec to sec
8. Recommended fuse (fuse on primary): For 115V - Cooper/Bussman, Type MDL, rated 500mA, 250V. For 230V – Littlefuse, Type 313, rated 250mA, 250V

Construction:

Three flange bobbin construction with primaries and secondaries wound side by side for low capacitive coupling. UL Class F Insulation System (155°C).

Agency File:

UL: File E65390, UL 5085-1 & 3 (1585), Class 2 not wet / Class 3 wet Transformer
cUL: File E65390, UL 5085-1 & 3 (1585) For Canadian Use (CSA 22.2, No.66.3-06)
TUV Certificate No.: R72120839, EN61558, Safety Isolating xfmr, general use

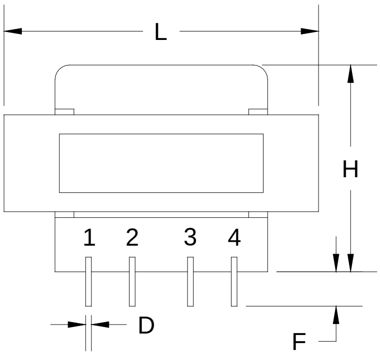


Dimensions:

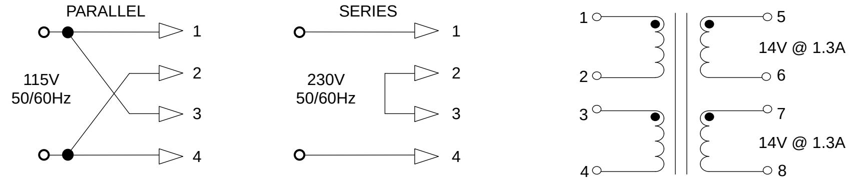
Units in inches.

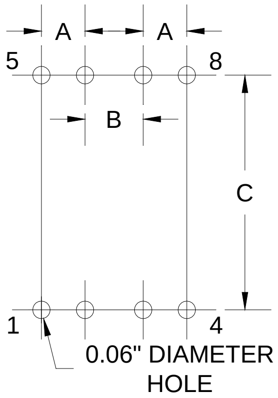
H	W	L	A	B	C	D	E	F
1.562	2.187	2.625	0.400	0.400	1.850	0.041	0.020	0.234

Weight: 1.10 lbs



Schematic:





Board Layout

RoHS Compliance: As of manufacturing date February 2005, all standard products meet the requirements of 2011/65/EU, known as the RoHS initiative.

Note: Order and shipping documentation may have a “-B” suffix; this indicates Bulk packaging but does not show on the actual part number marked on the transformer.

*Upon printing, this document is considered “uncontrolled”. Please contact Triad Magnetics website for the most current version. For soldering and washing information please see http://www.triadmagnetics.com/faq.html

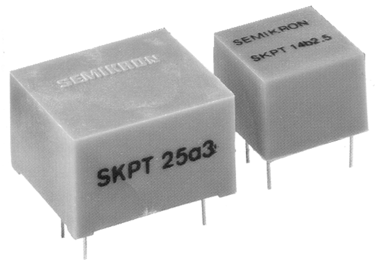
back zurück

14.2 Pulse Transformers

Range of preferred types

Pulse Transformers

SKPT 14 to SKPT 27



Absolute Maximum Ratings

Symbol	Conditions	Values
V_{ww}	Crest working voltage	400 ... 650 V
V_{isol}	A.C. rms; 1 minute, see table below 1)	2,5 ... 5 kV
T_{op}	Operating Temperature	– 40 ... + 85 °C
T_{stg}	Storage Temperature	– 50 ... + 90 °C

Characteristics 2)

Types	N_p/N_s	$\int V dt$	R_p	R_s	L_p	L_{ss}	C_{ps}	I_M	t_r	R_L	V_{ww}	V_{isol}	Win-ding
• New Type	s	µVs	Ω	Ω	mH	µH	pF	mA	µs	Ω	V	kV	conf
SKPT 14b2,5	1:1:1	250	0,86	0,86	1,8	85	10	150	2	80	500	4	B
SKPT 14k2,5	1:1:1	250	0,86	0,86	1,8	85	10	150	2	80	500	4	C
SKPT 14c2,5	2:1	250	1,6	0,86	7,5	400	12	150	2,5	80	500	4	D
SKPT 14a3	1:1	350	1,25	1,25	2,8	135	12	150	2,5	80	500	4	A
SKPT 14i3	1:1	350	1,25	1,25	2,8	135	12	150	2,5	80	500	4	D
SKPT 14g3	2:1:1	330	3,5	1,6	11	148	10	150	5	80	500	4	B
SKPT 14c3,5	2:1	350	3,5	2,4	13,5	82	9	150	2,5	80	500	4	D
SKPT 14i5	1:1	500	2,7	2,7	5,5	75	10	150	2,5	80	500	4	D
SKPT 14k6	1:1:1	600	2,8	2,8	9	290	10	150	2,5	80	500	4	C
SKPT 25j2	1:2:2	200	0,8	1,6	0,9/1,6	30/60	7	250	1,5	47	500	5	H
SKPT 25a3	1:1	300	0,55	0,55	2	45	8	250	1,5	47	500	4	A
SKPT 25b3	1:1:1	300	0,55	0,55	2	48	9	250	1,5	47	500	4	B
SKPT 25e3	3:1:1	300	1,7	0,55	15	300	10	250	1,5	47	500	4	B
SKPT 25h3	1:1:1:1	300	0,55	0,55	2	48	9	250	1,5	47	500	4	C
SKPT 25k3/650	1:1:1	300	0,55	0,55	2	38	9	250	1,5	47	650	4	F
SKPT 25m3	1:1	300	0,55	0,55	1,8	105	7	250	1,5	47	1000	6	G
SKPT 25n3	3:1	300	1,7	0,55	15	870	7	250	1,5	47	1000	6	G
SKPT 25p3/650	3:1:1	300	1,7	0,55	15	300	10	250	1,5	47	650	4	F
SKPT 25a4	1:1	400	0,6	0,6	4	50	10	250	2	47	500	4	A
SKPT 25b4	1:1:1	400	0,6	0,6	4	52	10	250	2	47	500	4	B
SKPT 25g4	2:1:1	400	2,3	1,1	9/15	260/490	7	250	1,5	47	500	5	H
SKPT 25a5	1:1	500	1	1	5,5	85	11	100 250	1,1 3	100 47	500	4	A

continued on next page

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1) Material used is according to UL94-V0. Isolation test and pin distance according to IEC 60664-1(1992); (VDE 0110-1:1997-4)

2) Explanations see Chapter A, Section 14.2

14.2 Pulse Transformers (continued)

Types	**N_p/N_s**	$\int$Vdt	**R_p**	**R_s**	**L_p**	**L_{ss}**	**C_{ps}**	**I_M**	**t_r**	**R_L**	**V_{ww}**	**V_{isol}**	**Win-ding**
• New Type	**s**	**µVs**	**Ω**	**Ω**	**mH**	**µH**	**pF**	**mA**	**µs**	**Ω**	**V**	**kV**	**conf**
SKPT 25b5	1:1:1	500	1	1	5,5	89	12	100 250	1,1 3	100 47	500	4	B
SKPT 25m5	1:1	500	1	1	5,5	170	7	250	1,5	47	1000	6	G
SKPT 25o5	2:1	500	2,1	1	32	830	7,5	250	1,5	47	1000	5	G
SKPT 25b8	1:1:1	800	1,6	1,6	14	220	14	25 250	1 6	470 47	500	4	B
SKPT 25b10	1:1:1	1000	1,8	1,8	18	260	13	25 250	1 6	470 47	500	4	B
SKPT 26a3	1:1	300	0,55	0,55	2	45	8	250	1,5	47	500	4	A
SKPT 26b3	1:1:1	300	0,55	0,55	2	48	8	250	1,5	47	500	4	B
SKPT 26e3	3:1:1	300	1,7	0,55	15	300	10	250	1,5	47	500	4	B
SKPT 26b10	1:1:1	1000	1,8	1,8	18	260	15	25 250	1 6	470 47	500	4	B
SKPT 21a3	1:1	270	0,6	0,6	3,5	3,5	55	800	0,8	15	650	4	A
SKPT 21b3	1:1:1	270	0,6	0,6	3,5	3,5	55	800	0,8	15	440	2,5	B
SKPT 21b3/650	1:1:1	270	0,6	0,5/0,7	3,5	2,7/3,2	30	800	0,8	15	650	4	B
SKPT 21c3	2:1	275	1,0	0,6	6,5	10	50	800	0,8	15	650	4	A
SKPT 21d3	3:1	270	1,5	0,6	30	20	65	800	0,8	15	650	4	A
SKPT 21e3	3:1:1	270	1,5	0,6	30	20	65	800	0,8	15	440	2,5	B
SKPT 21b4	1:1:1	370	0,7	0,7	6	3,5	65	800	0,8	15	440	2,5	B
SKPT 21b4/650	1:1:1	370	0,7	0,6/0,8	6	4,3/7	65	800	0,8	15	650	4	B
SKPT 21a5	1:1	450	1,0	1,0	10	10	65	800	0,8	15	650	4	A
SKPT 21b5	1:1:1	450	1,0	1,0	10	4,5	65	800	0,8	15	440	2,5	B
SKPT 21b5/650	1:1:1	450	1,0	1,0	10	10	65	800	0,8	15	650	4	B
SKPT 22e3/650	3:1:1	280	1,2	0,5	35	10	40	800	0,8	47	650	4	B
SKPT 27a3	1:1	300	0,3	0,3	2	3	76	1200	1	10	650	4	A
SKPT 27b3	1:1:1	300	0,3	0,3	2	3	95	1200	1	10	500	3	B
SKPT 27b3/650	1:1:1	300	0,3	0,2/0,4	2	3	65	1200	1	10	650	4	B
SKPT 27d3,5	3:1	350	0,6	0,3	20	22	100	2500	1	4,7	650	4	A
SKPT 27e3,5	3:1:1	350	0,6	0,3	20	25	110	2500	1	4,7	650	4	B
SKPT 27b4/1300	1:1:1	450	0,1	0,1	0,55	7,5	8,5	2000	0,5	10	1300	6	B
SKPT 27a5	1:1	500	0,4	0,4	5	5	105	2000	1	10	650	4	A

continued on next page

[1] Material used is according to UL94-V0. Isolation test and pin distance according to IEC 60664-1(1992); (VDE 0110-1:1997-4)

[2] Explanations see Chapter A, Section 14.2

14.2 Pulse Transformers (continued)

Types	N_p/N_s	$\int V dt$	R_p	R_s	L_p	L_{ss}	C_{ps}	I_M	t_r	R_L	V_{ww}	V_{isol}	Winding
• New Type	s	µVs	Ω	Ω	mH	µH	pF	mA	µs	Ω	V	kV	conf
SKPT 27b5	1:1:1	500	0,4	0,4	5	5	117	2000	1	10	500	3	B
SKPT 27b5/650	1:1:1	500	0,4	0,3/0,5	5	5	100	2000	1	10	650	4	B
SKPT 27a10	1:1	1000	0,3	0,3	2,5	5	83	2000	1	10	650	4	A
SKPT 27b10	1:1:1	1000	0,3	0,3	2,5	5	97	2000	1	10	500	3	B
SKPT 27b10/650	1:1:1	1000	0,3	0,2/0,4	2,5	5	84	2000	1	10	650	4	B
SKPT 27b10ES	1:1:1	1000	0,3	0,3	2,5	5	97	2000	1	10	650	4	C
SKPT 27c10	2:1	1000	0,5	0,3	10	15	110	2000	1	10	650	4	A
SKPT HVb3	1:1:1	300	0,3	0,3	3	75	8,5	1000	1	50	3200	12	A
SKPT 25a3/s	1:1	300	0,55	0,55	2	12	20	250	0,8	47	440	3	A
SKPT 25b3/s	1:1:1	300	0,55	0,55	2	12	20	250	0,8	47	440	3	B
SKPT 25e3/s	3:1:1	300	1,8	0,8	15	80	28	250	0,8	47	440	3	B
SKPT 25h3/s	1:1:1:1	300	0,55	0,55	2	12	20	250	0,8	47	440	3	C
SKPT 25a4/s	1:1	400	0,8	0,9	4	17	28	250	0,8	47	440	3	A
SKPT 909	1:1	400	0,8	0,9	4	17	28	600	1	5	900	3	E
SKPT 25b4/s	1:1:1	400	0,8	0,9	4	17	28	250	0,8	47	500	3	B
SKPT 25b4/hs	1:1:1	400	0,8	0,9	1,8	15	28	250	0,8	400	700	4	D
SKPT 25a5/s	1:1	500	1	1,1	5,5	22	28	100 250	0,8 1	100 47	500	3	A
SKPT 25b5/s	1:1:1	500	1,1	1,2	5,5	25	30	100 250	0,8 1	100 47	500	3	B
SKPT 25b6/N	1:1:1	650	1,13	1,2	4,6	20	37	250	1	47	600	4	B
SKPT 25b8/s	1:1:1	800	1,8	2,1	14	40	35	25 250	0,8 1,5	470 47	500	3	B
SKPT 25b10/s	1:1:1	1000	2,2	2,4	18	50	40	25 250	0,8 1,5	470 47	500	3	B
SKPT 25b20/s	1:1:1	2000	6	6	55	100	45	250	3	47	500	3	B

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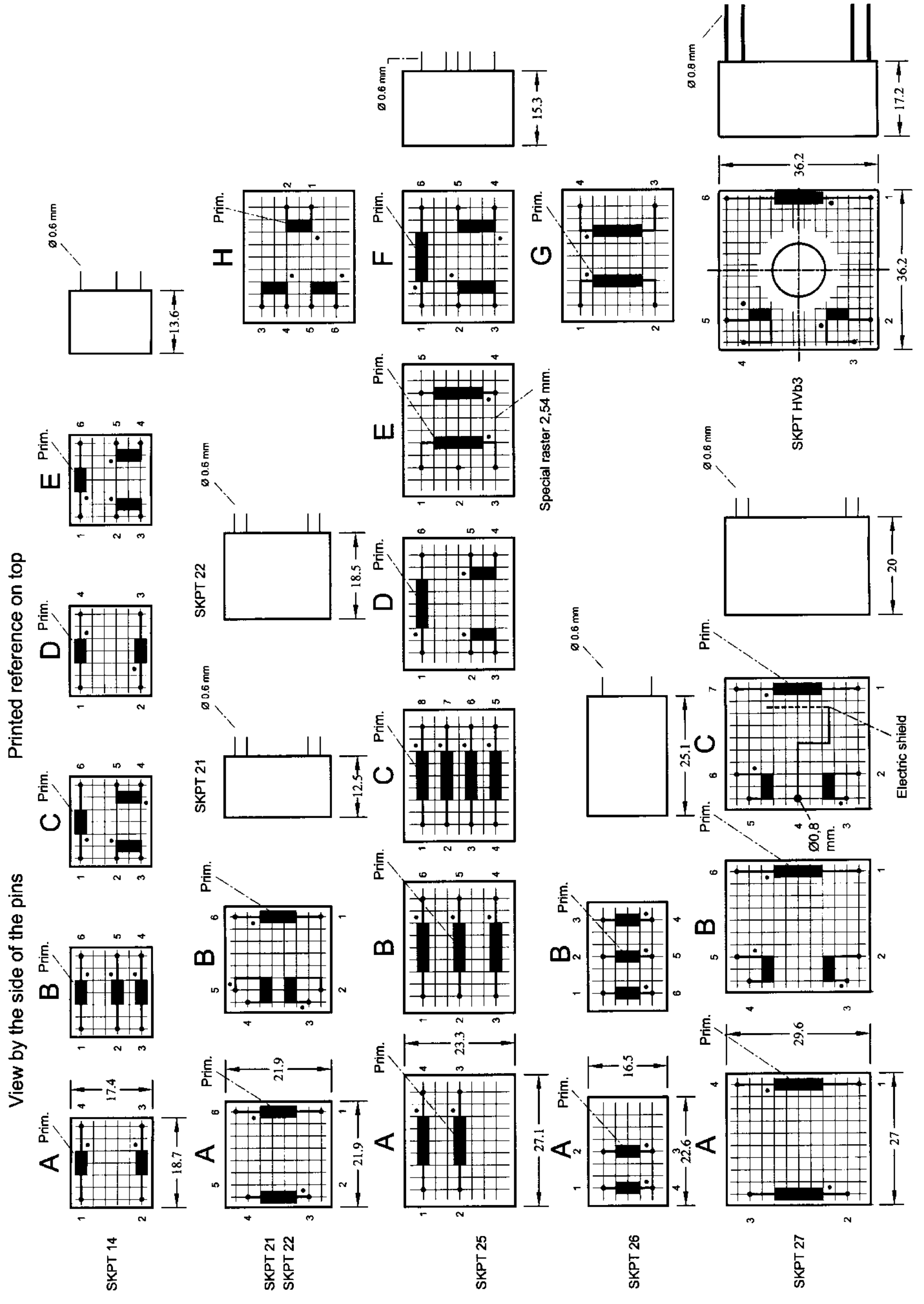
[1] Material used is according to UL94-V0. Isolation test and pin distance according to IEC 60664-1(1992); (VDE 0110-1:1997-4)

[2] Explanations see Chapter A, Section 14.2

Winding Configurations and Dimensions in mm
2,5 mm grid



Current Transformer
TI 300/0,3
300 A / 0,3 A

Absolute Maximum Ratings

Symbol	**Term**	**Values**
I_1	Max. primary current	300 A
I_2	Max. secondary current	0,3 A
	Precision class sec. current	0,5 %
$\frac{n_s}{n_p}$	Transformer current ratio	1000 : 1
P_{out}	Max. Power output (50/60 Hz)	2 VA
f_{op}	Operating frequency	50 / 60 Hz
R_2	Load resistance 1)	> 22,2 Ω

TI 300 / 0,3

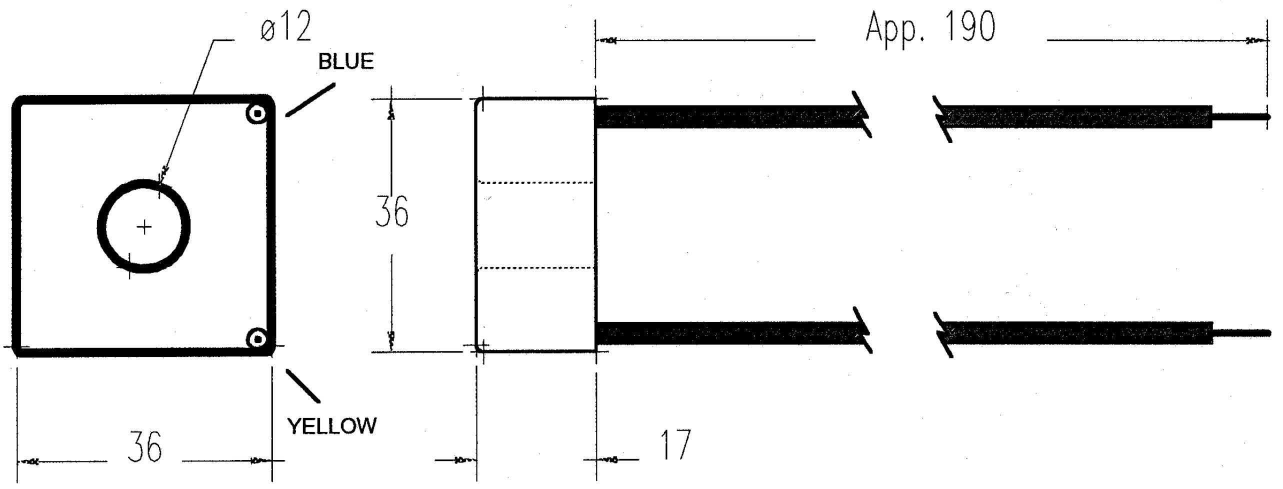


Fig. 1 Outline

Dimensions in mm

LM555 Timer

1 Features

- Direct Replacement for SE555/NE555
- Timing from Microseconds through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- Output Can Source or Sink 200 mA
- Output and Supply TTL Compatible
- Temperature Stability Better than 0.005% per °C
- Normally On and Normally Off Output
- Available in 8-pin VSSOP Package

2 Applications

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Linear Ramp Generator

3 Description

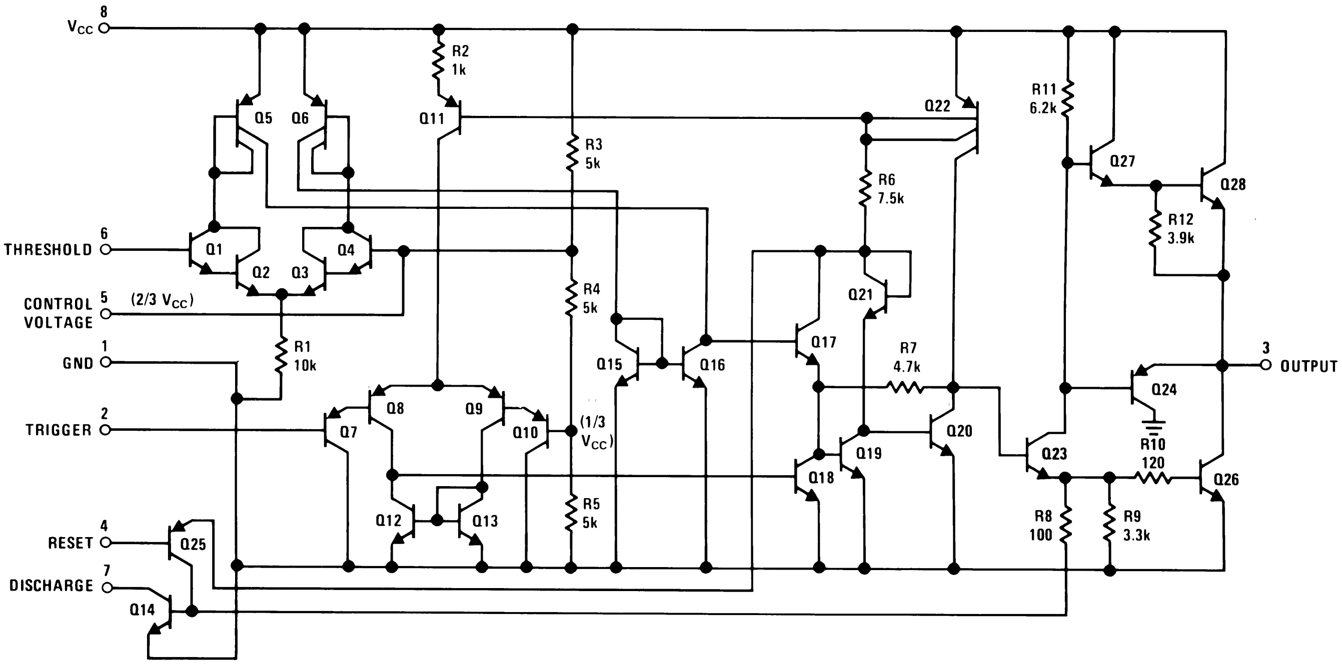
The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM555	SOIC (8)	4.90 mm × 3.91 mm
	PDIP (8)	9.81 mm × 6.35 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Schematic Diagram



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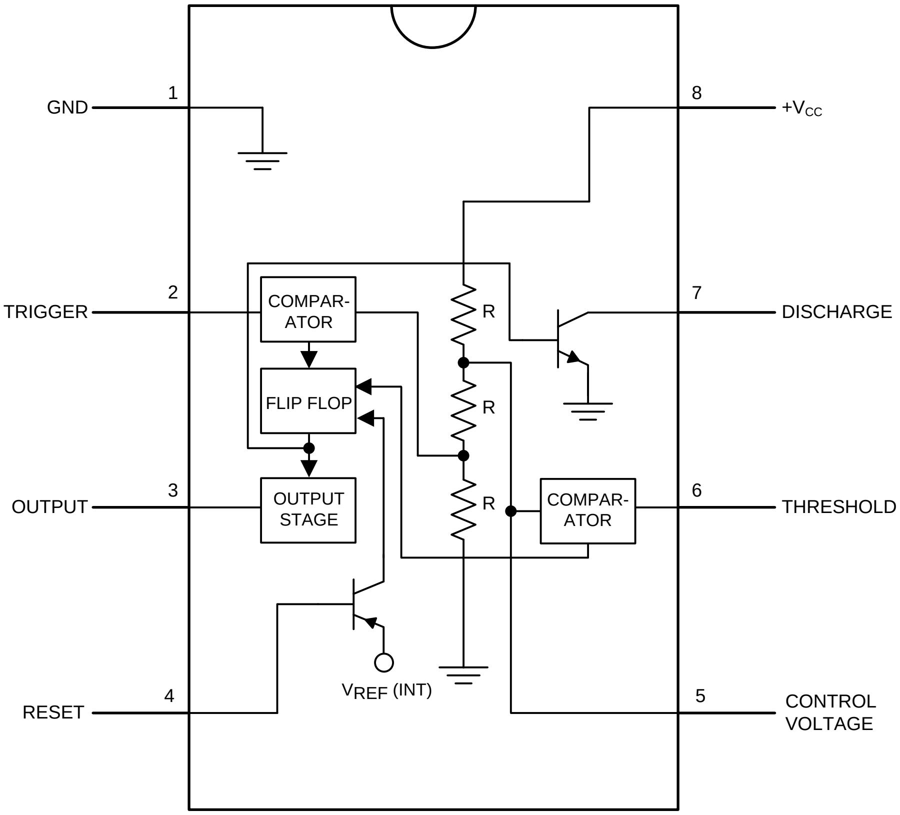
4 Revision History

Changes from Revision C (March 2013) to Revision D	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	13

5 Pin Configuration and Functions

D, P, and DGK Packages
8-Pin PDIP, SOIC, and VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
5	Control Voltage	I	Controls the threshold and trigger levels. It determines the pulse width of the output waveform. An external voltage applied to this pin can also be used to modulate the output waveform
7	Discharge	I	Open collector output which discharges a capacitor between intervals (in phase with output). It toggles the output from high to low when voltage reaches 2/3 of the supply voltage
1	GND	O	Ground reference voltage
3	Output	O	Output driven waveform
4	Reset	I	Negative pulse applied to this pin to disable or reset the timer. When not used for reset purposes, it should be connected to VCC to avoid false triggering
6	Threshold	I	Compares the voltage applied to the terminal with a reference voltage of 2/3 Vcc. The amplitude of voltage applied to this terminal is responsible for the set state of the flip-flop
2	Trigger	I	Responsible for transition of the flip-flop from set to reset. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin
8	V^+	I	Supply voltage with respect to GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
Power Dissipation(3)		LM555CM, LM555CN(4)		1180	mW
		LM555CMM		613	mW
Soldering Information	PDIP Package	Soldering (10 Seconds)		260	°C
	Small Outline Packages (SOIC and VSSOP)	Vapor Phase (60 Seconds)		215	°C
		Infrared (15 Seconds)		220	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) For operating at elevated temperatures the device must be derated above 25°C based on a 150°C maximum junction temperature and a thermal resistance of 106°C/W (PDIP), 170°C/W (S0IC-8), and 204°C/W (VSSOP) junction to ambient.
(4) Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500(2)	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The ESD information listed is for the SOIC package.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage		18	V
Temperature, T_A	0	70	°C
Operating junction temperature, T_J		70	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM555			UNIT
		PDIP	SOIC	VSSOP	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106	170	204	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

(T_A = 25°C, V_{CC} = 5 V to 15 V, unless otherwise specified)(1)(2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage		4.5		16	V
Supply Current	V_{CC} = 5 V, R_L = ∞		3	6	mA
	V_{CC} = 15 V, R_L = ∞ (Low State) (3)		10	15	
Timing Error, Monostable					
Initial Accuracy			1 %		
Drift with Temperature	R_A = 1 k to 100 kΩ,		50		ppm/°C
	C = 0.1 μF, (4)				
Accuracy over Temperature			1.5 %		
Drift with Supply			0.1 %		V
Timing Error, Astable					
Initial Accuracy			2.25		
Drift with Temperature	R_A, R_B =1 k to 100 kΩ,		150		ppm/°C
	C = 0.1 μF, (4)				
Accuracy over Temperature			3.0%		
Drift with Supply			0.30 %		/V
Threshold Voltage			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15 V		5		V
	V_{CC} = 5 V		1.67		V
Trigger Current			0.5	0.9	μA
Reset Voltage		0.4	0.5	1	V
Reset Current			0.1	0.4	mA
Threshold Current	(5)		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15 V	9	10	11	V
	V_{CC} = 5 V	2.6	3.33	4	
Pin 7 Leakage Output High			1	100	nA
Pin 7 Sat (6)					
Output Low	V_{CC} = 15 V, I_7 = 15 mA		180		mV
Output Low	V_{CC} = 4.5 V, I_7 = 4.5 mA		80	200	mV
Output Voltage Drop (Low)	V_{CC} = 15 V				
	I_{SINK} = 10 mA		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.5	V
	I_{SINK} = 200 mA		2.5		V
	V_{CC} = 5 V				
	I_{SINK} = 8 mA				V
	I_{SINK} = 5 mA		0.25	0.35	V

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensures specific performance limits. This assumes that the device is within the *Recommended Operating Conditions*. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Supply current when output high typically 1 mA less at V_{CC} = 5 V.
(4) Tested at V_{CC} = 5 V and V_{CC} = 15 V.
(5) This will determine the maximum value of R_A + R_B for 15 V operation. The maximum total (R_A + R_B) is 20 MΩ.
(6) No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Electrical Characteristics (continued)

(T_A = 25°C, V_{CC} = 5 V to 15 V, unless otherwise specified)(1)(2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15 V		12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15 V	12.75	13.3		V
	V_{CC} = 5 V	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

6.6 Typical Characteristics

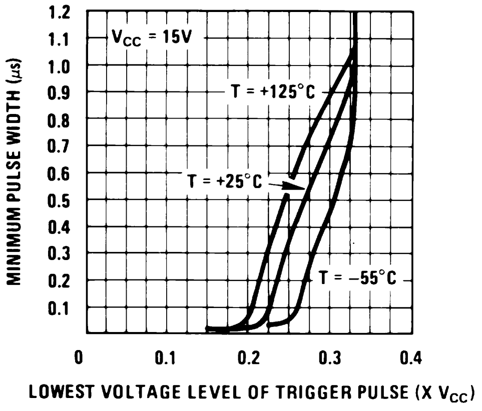


Figure 1. Minimum Pulse Width Required For Triggering

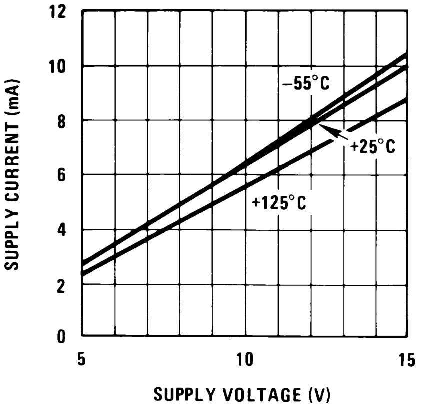


Figure 2. Supply Current vs. Supply Voltage

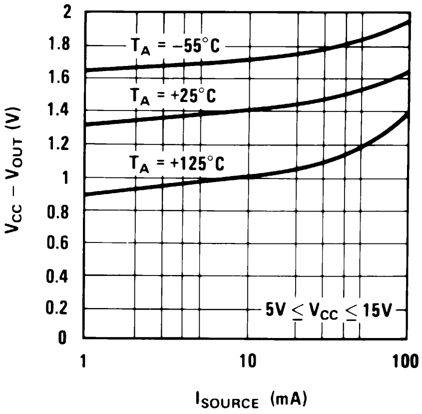


Figure 3. High Output Voltage vs. Output Source Current

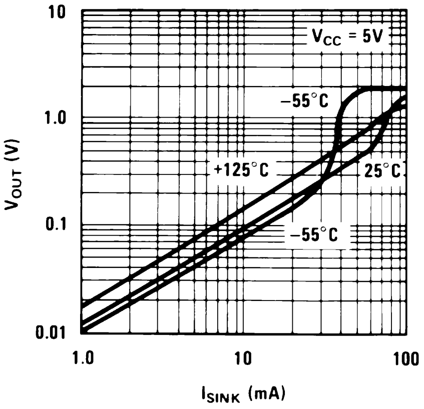


Figure 4. Low Output Voltage vs. Output Sink Current

Typical Characteristics (continued)

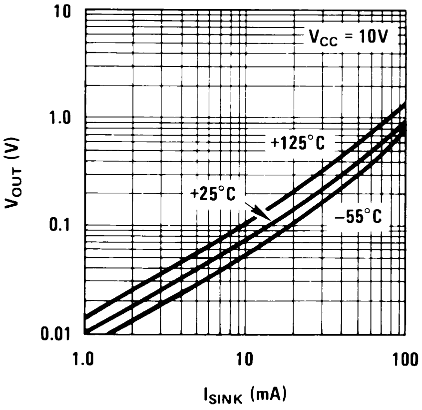


Figure 5. Low Output Voltage vs. Output Sink Current

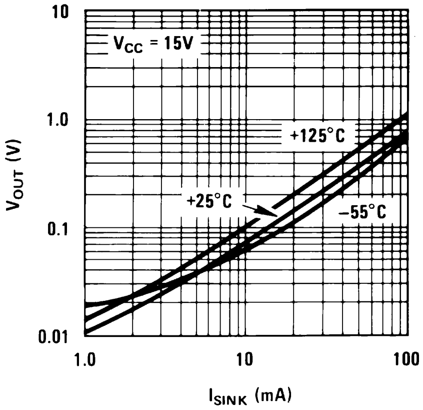


Figure 6. Low Output Voltage vs. Output Sink Current

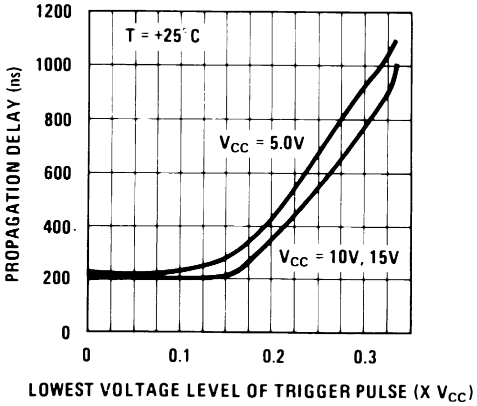


Figure 7. Output Propagation Delay vs. Voltage Level of Trigger Pulse

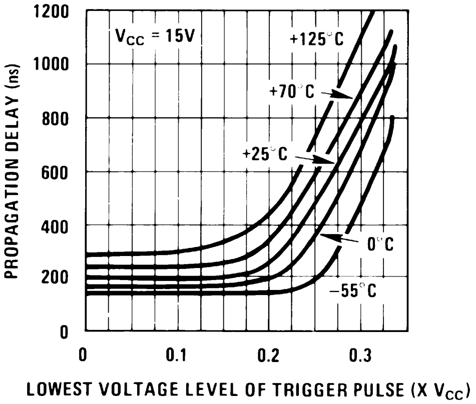


Figure 8. Output Propagation Delay vs. Voltage Level of Trigger Pulse

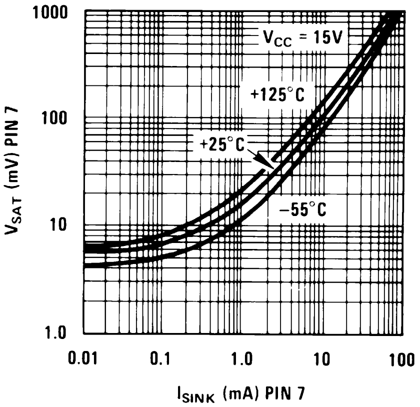


Figure 9. Discharge Transistor (Pin 7) Voltage vs. Sink Current

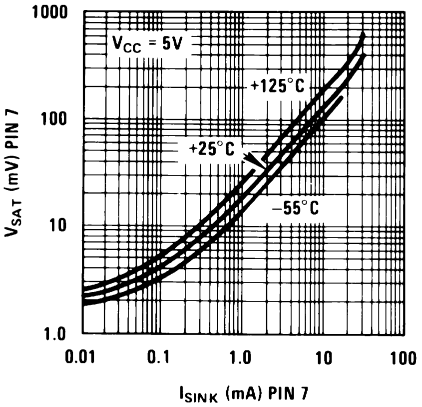


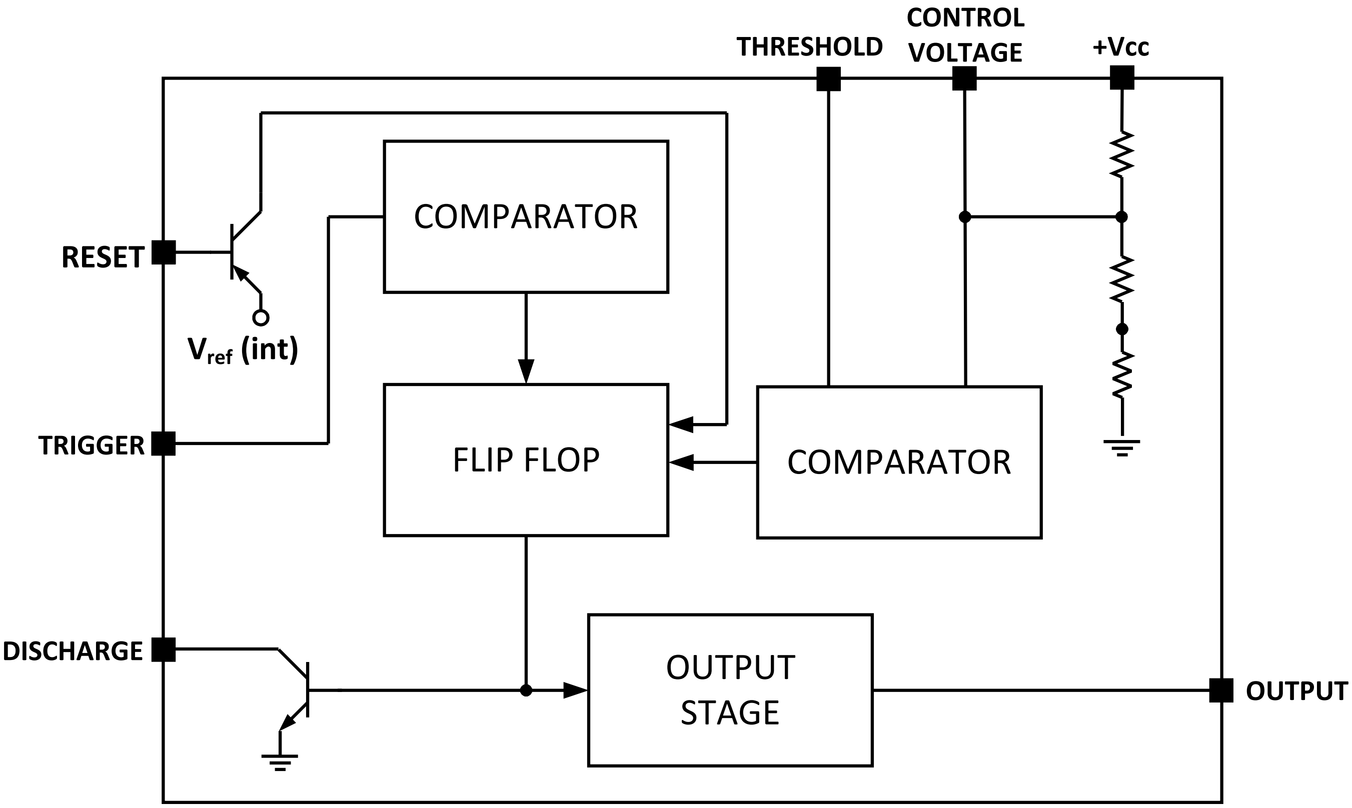
Figure 10. Discharge Transistor (Pin 7) Voltage vs. Sink Current

7 Detailed Description

7.1 Overview

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or driver TTL circuits. The LM555 are available in 8-pin PDIP, SOIC, and VSSOP packages and is a direct replacement for SE555/NE555.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Direct Replacement for SE555/NE555

The LM555 timer is a direct replacement for SE555 and NE555. It is pin-to-pin compatible so that no schematic or layout changes are necessary. The LM555 come in an 8-pin PDIP, SOIC, and VSSOP package.

7.3.2 Timing From Microseconds Through Hours

The LM555 has the ability to have timing parameters from the microseconds range to hours. The time delay of the system can be determined by the time constant of the R and C value used for either the monostable or astable configuration. A nomograph is available for easy determination of R and C values for various time delays.

7.3.3 Operates in Both Astable and Monostable Mode

The LM555 can operate in both astable and monostable mode depending on the application requirements.

- Monostable mode: The LM555 timer acts as a “one-shot” pulse generator. The pulse beings when the LM555 timer receives a signal at the trigger input that falls below a 1/3 of the voltage supply. The width of the output pulse is determined by the time constant of an RC network. The output pulse ends when the voltage on the

Feature Description (continued)

capacitor equals 2/3 of the supply voltage. The output pulse width can be extended or shortened depending on the application by adjusting the R and C values.

- Astable (free-running) mode: The LM555 timer can operate as an oscillator and puts out a continuous stream of rectangular pulses having a specified frequency. The frequency of the pulse stream depends on the values of R_A, R_B, and C.

7.4 Device Functional Modes

7.4.1 Monostable Operation

In this mode of operation, the timer functions as a one-shot (Figure 11). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

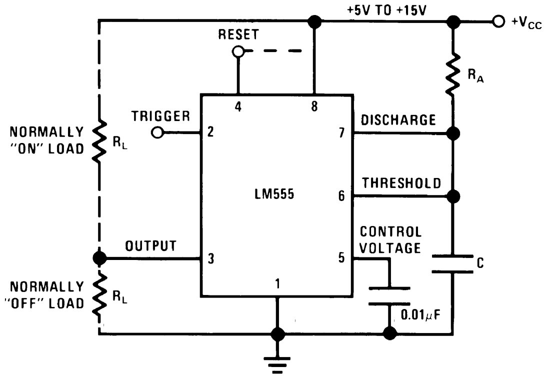
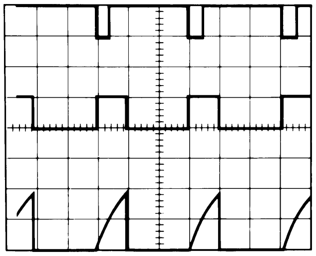


Figure 11. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. Figure 12 shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



V_{CC} = 5 V
TIME = 0.1 ms/DIV.
R_A = 9.1 kΩ
C = 0.01 μF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

Figure 12. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10 μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, TI recommends connecting the Reset pin to V_{CC} to avoid any possibility of false triggering.

Device Functional Modes (continued)

Figure 13 is a nomograph for easy determination of R, C values for various time delays.

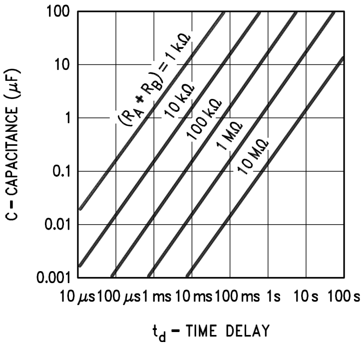


Figure 13. Time Delay

7.4.2 Astable Operation

If the circuit is connected as shown in Figure 14 (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

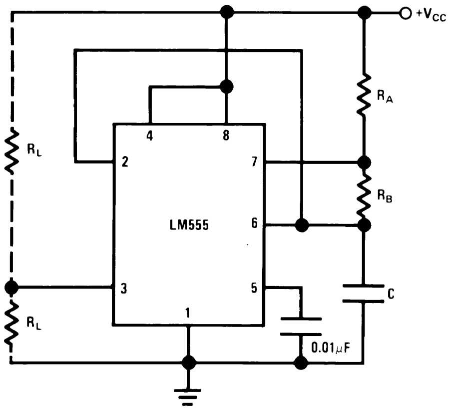
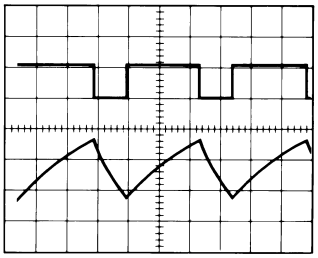


Figure 14. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 15 shows the waveforms generated in this mode of operation.

Device Functional Modes (continued)



V_{CC} = 5 V
TIME = 20µs/DIV.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 µF

Top Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

Figure 15. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C \tag{1}$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C \tag{2}$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C \tag{3}$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2\,R_B)\,C} \tag{4}$$

Figure 16 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B} \tag{5}$$

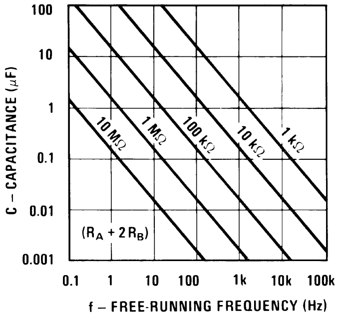


Figure 16. Free Running Frequency

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM555 timer can be used a various configurations, but the most commonly used configuration is in monostable mode. A typical application for the LM555 timer in monostable mode is to turn on an LED for a specific time duration. A pushbutton is used as the trigger to output a high pulse when trigger pin is pulsed low. This simple application can be modified to fit any application requirement.

8.2 Typical Application

Figure 17 shows the schematic of the LM555 that flashes an LED in monostable mode.

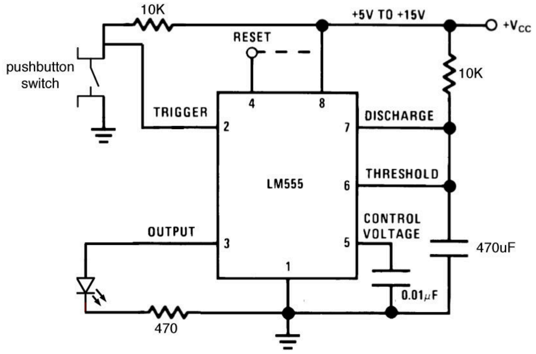


Figure 17. Schematic of Monostable Mode to Flash an LED

8.2.1 Design Requirements

The main design requirement for this application requires calculating the duration of time for which the output stays high. The duration of time is dependent on the R and C values (as shown in Figure 17) and can be calculated by:

$$t = 1.1 \times R \times C \text{ seconds} \quad (6)$$

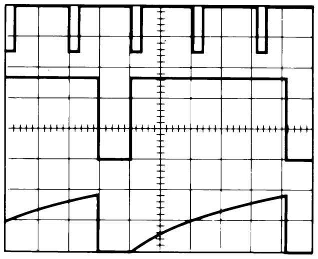
8.2.2 Detailed Design Procedure

To allow the LED to flash on for a noticeable amount of time, a 5 second time delay was chosen for this application. By using Equation 6, RC equals 4.545. If R is selected as 100 kΩ, C = 45.4 µF. The values of R = 100 kΩ and C = 47 µF was selected based on standard values of resistors and capacitors. A momentary push button switch connected to ground is connected to the trigger input with a 10-K current limiting resistor pullup to the supply voltage. When the push button is pressed, the trigger pin goes to GND. An LED is connected to the output pin with a current limiting resistor in series from the output of the LM555 to GND. The reset pin is not used and was connected to the supply voltage.

8.2.2.1 Frequency Divider

The monostable circuit of Figure 11 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 18 shows the waveforms generated in a divide by three circuit.

Typical Application (continued)



V_{CC} = 5 V Top Trace: Input 4 V/Div.
TIME = 20 μs/DIV. Middle Trace: Output 2V/Div.
R_A = 9.1 kΩ Bottom Trace: Capa citor 2V/Div.
C = 0.01 μF

Figure 18. Frequency Divider

8.2.2.2 Additional Information

Lower comparator storage time can be as long as 10 μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10 μs minimum.

Delay time reset to output is 0.47 μs typical. Minimum reset pulse width must be 0.3 μs, typical.

Pin 7 current switches within 30 ns of the output (pin 3) voltage.

8.2.3 Application Curves

The data shown below was collected with the circuit used in the typical applications section. The LM555 was configured in the monostable mode with a time delay of 5.17 s. The waveforms correspond to:

- Top Waveform (Yellow) – Capacitor voltage
- Middle Waveform (Green) – Trigger
- Bottom Waveform (Purple) – Output

As the trigger pin pulses low, the capacitor voltage starts charging and the output goes high. The output goes low as soon as the capacitor voltage reaches 2/3 of the supply voltage, which is the time delay set by the R and C value. For this example, the time delay is 5.17 s.

Typical Application (continued)

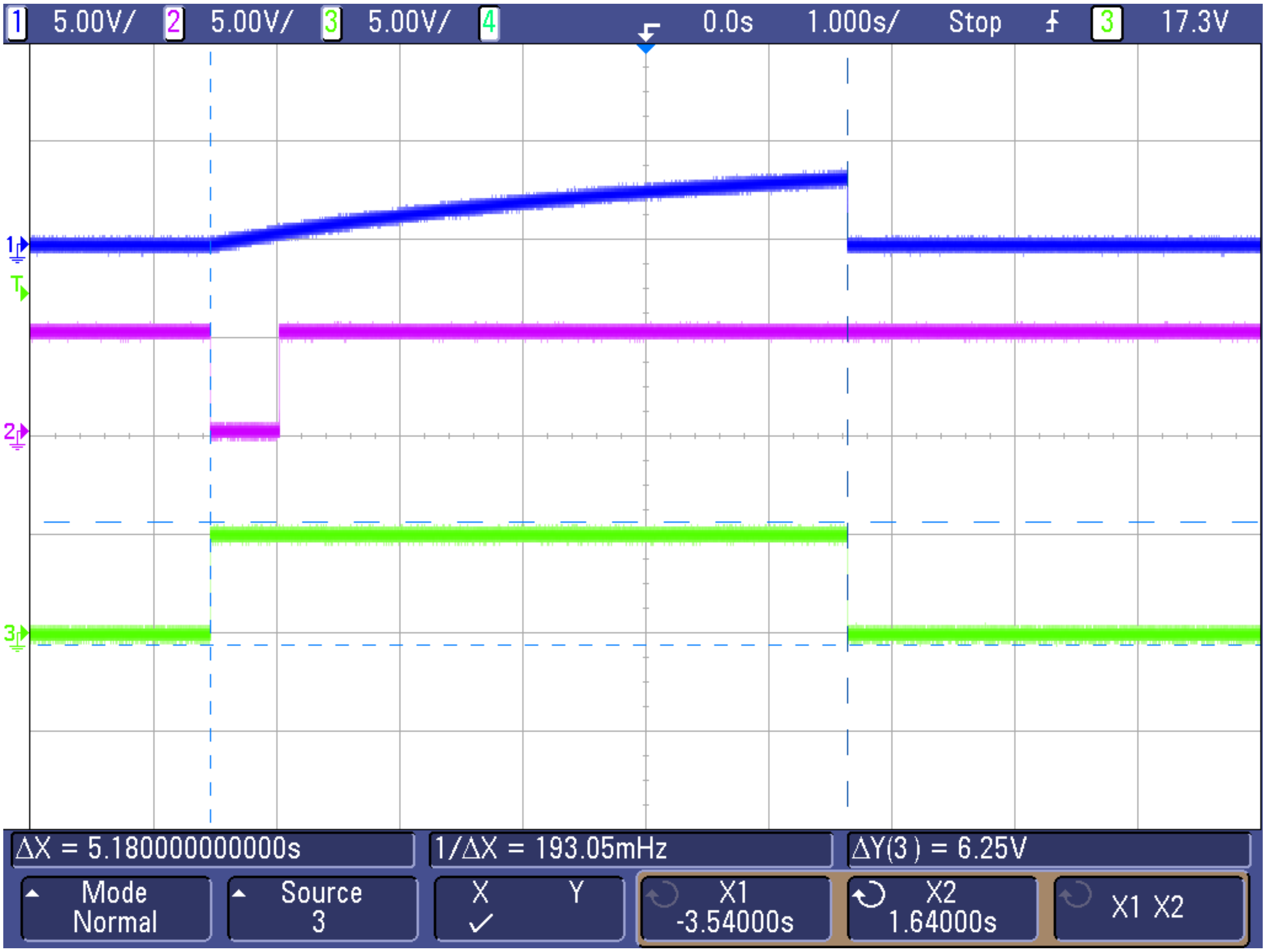


Figure 19. Trigger, Capacitor Voltage, and Output Waveforms in Monostable Mode

9 Power Supply Recommendations

The LM555 requires a voltage supply within 4.5 V to 16 V. Adequate power supply bypassing is necessary to protect associated circuitry. The minimum recommended capacitor value is 0.1 µF in parallel with a 1-µF electrolytic capacitor. Place the bypass capacitors as close as possible to the LM555 and minimize the trace length.

10 Layout

10.1 Layout Guidelines

Standard PCB rules apply to routing the LM555. The 0.1-µF capacitor in parallel with a 1-µF electrolytic capacitor should be as close as possible to the LM555. The capacitor used for the time delay should also be placed as close to the discharge pin. A ground plane on the bottom layer can be used to provide better noise immunity and signal integrity.

Figure 20 is the basic layout for various applications.

- C1 – based on time delay calculations
- C2 – 0.01-µF bypass capacitor for control voltage pin
- C3 – 0.1-µF bypass ceramic capacitor
- C4 – 1-µF electrolytic bypass capacitor
- R1 – based on time delay calculations
- U1 – LMC555

10.2 Layout Example

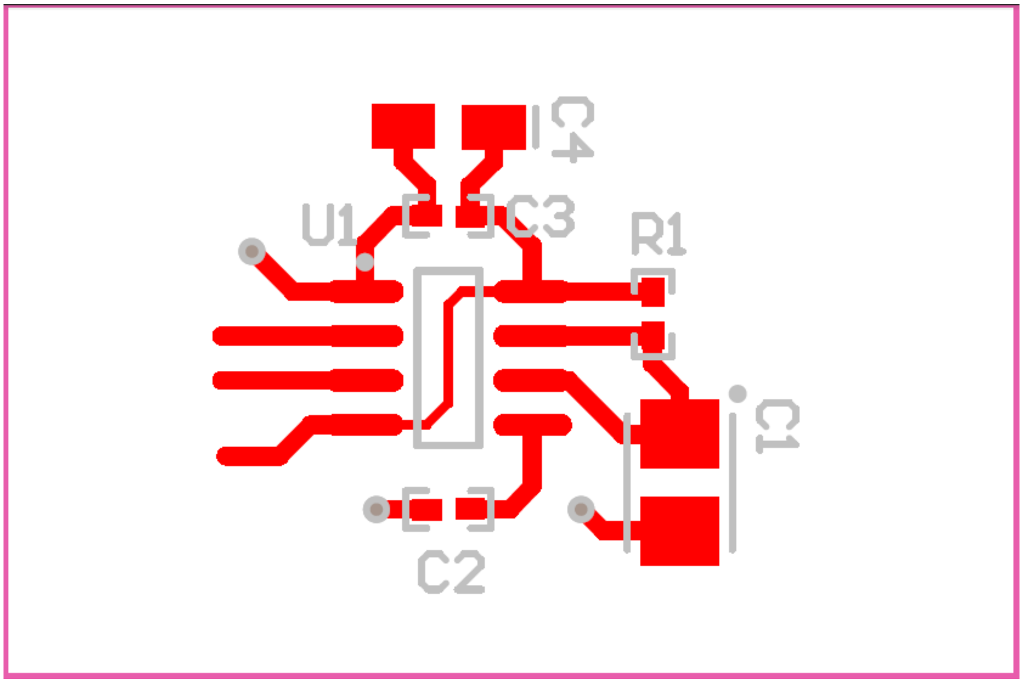


Figure 20. Layout Example

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM555-MWC	ACTIVE	WAFERSALE	YS	0	1	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-40 to 85		Samples
LM555CM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	LM 555CM	
LM555CM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM 555CM	Samples
LM555CMM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	0 to 70	Z55	
LM555CMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	Z55	Samples
LM555CMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	Z55	Samples
LM555CMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	LM 555CM	
LM555CMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM 555CM	Samples
LM555CN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LM 555CN	Samples
MC1455P1	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	0 to 70	LM 555CN	
NE555V	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	0 to 70	LM 555CN	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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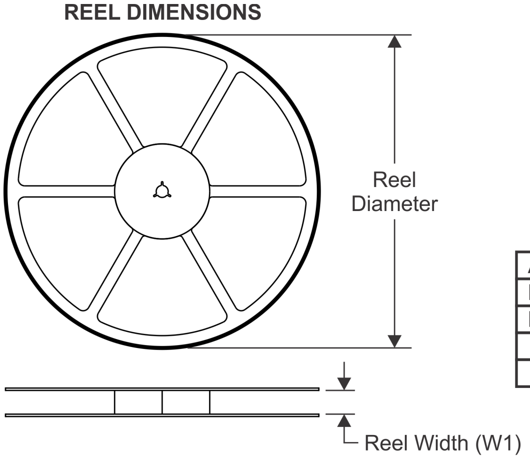
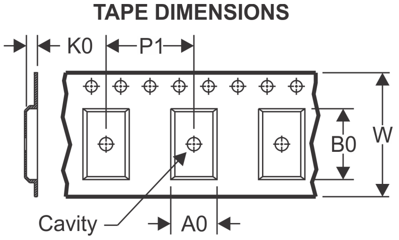
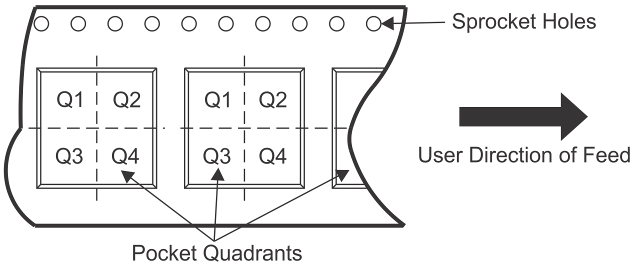
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

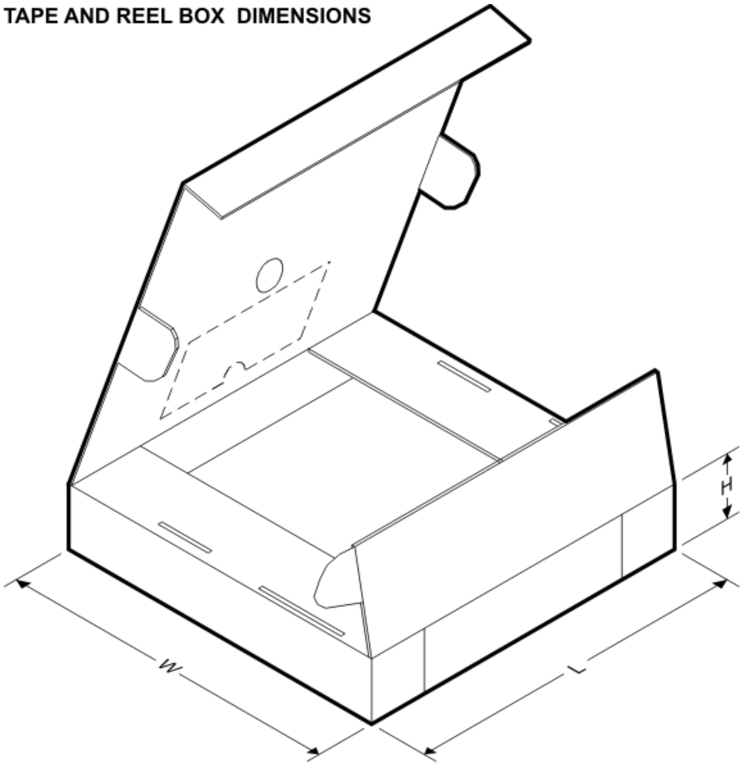
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM555CMM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM555CMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM555CMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM555CMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM555CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

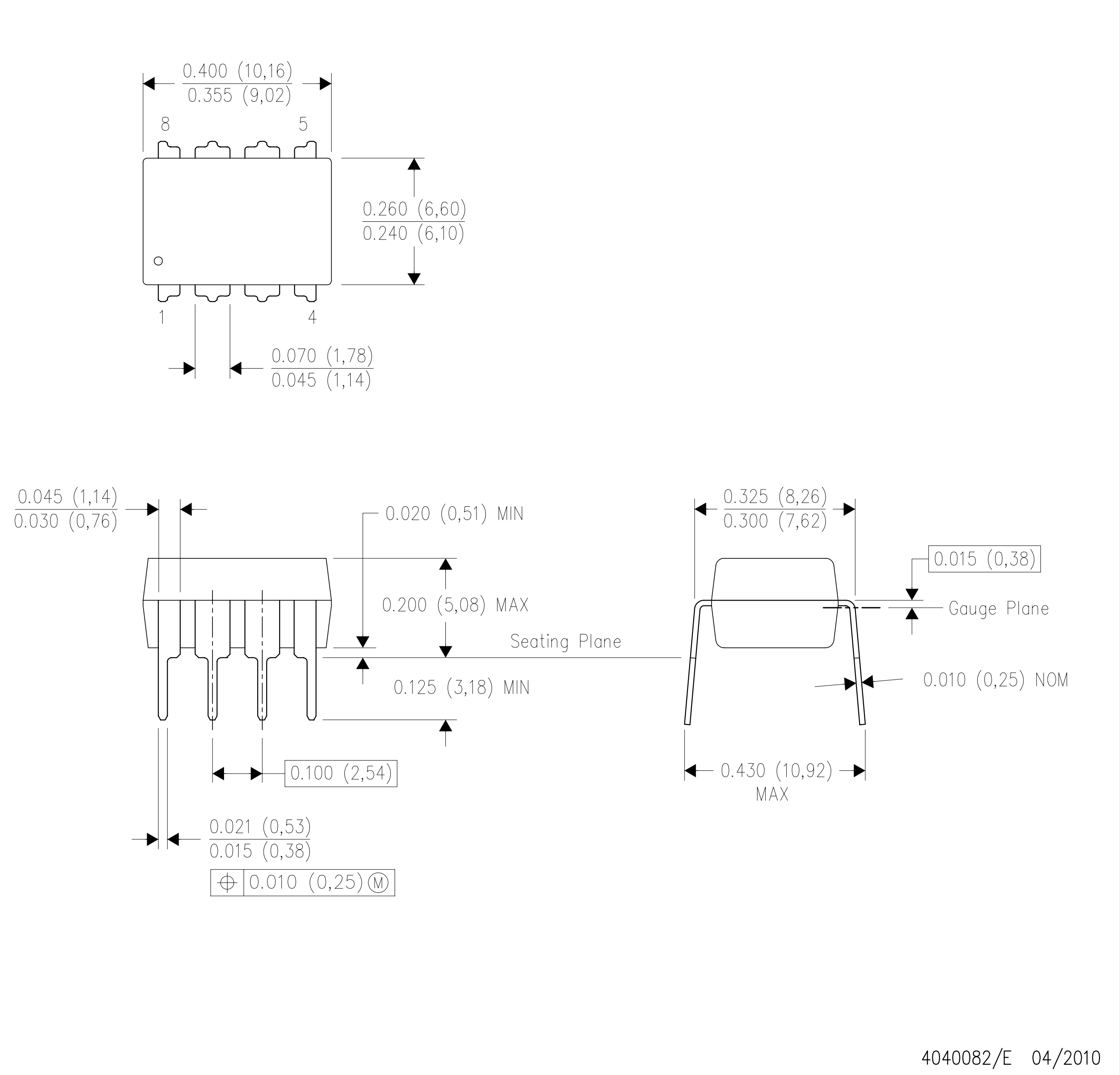
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

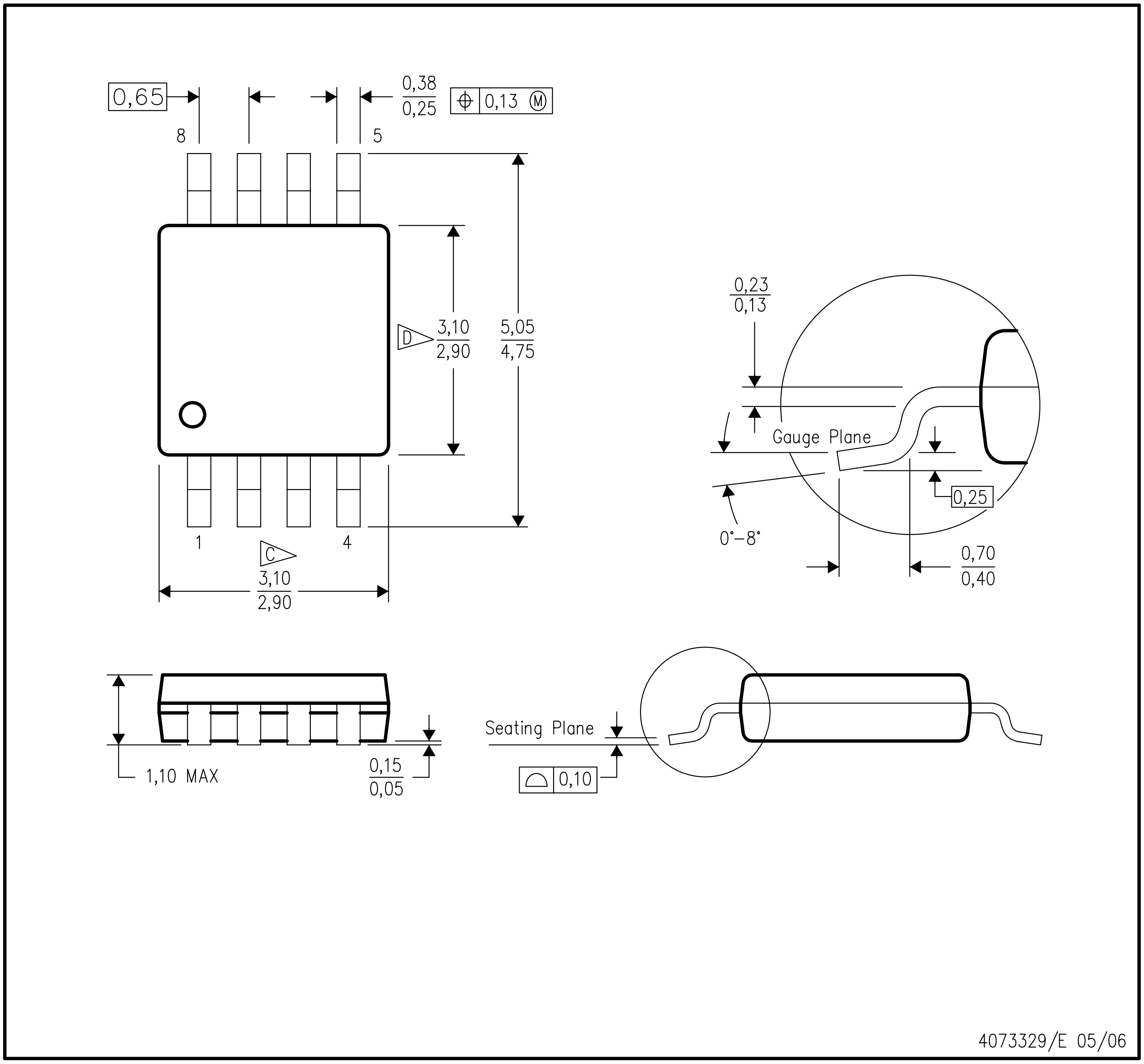
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM555CMM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM555CMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM555CMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM555CMX	SOIC	D	8	2500	367.0	367.0	35.0
LM555CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

P (R-PDIP-T8) PLASTIC DUAL-IN-LINE PACKAGE



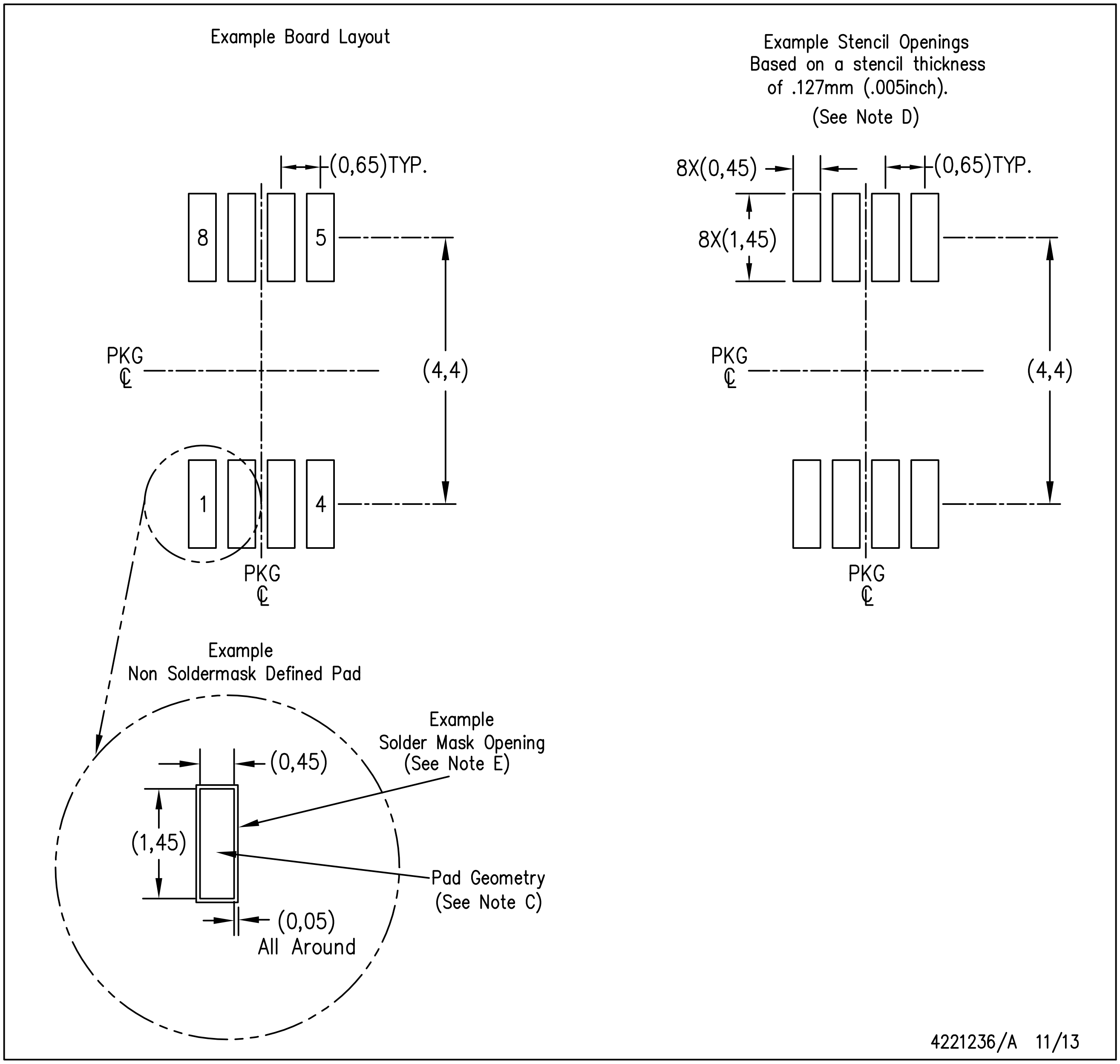
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



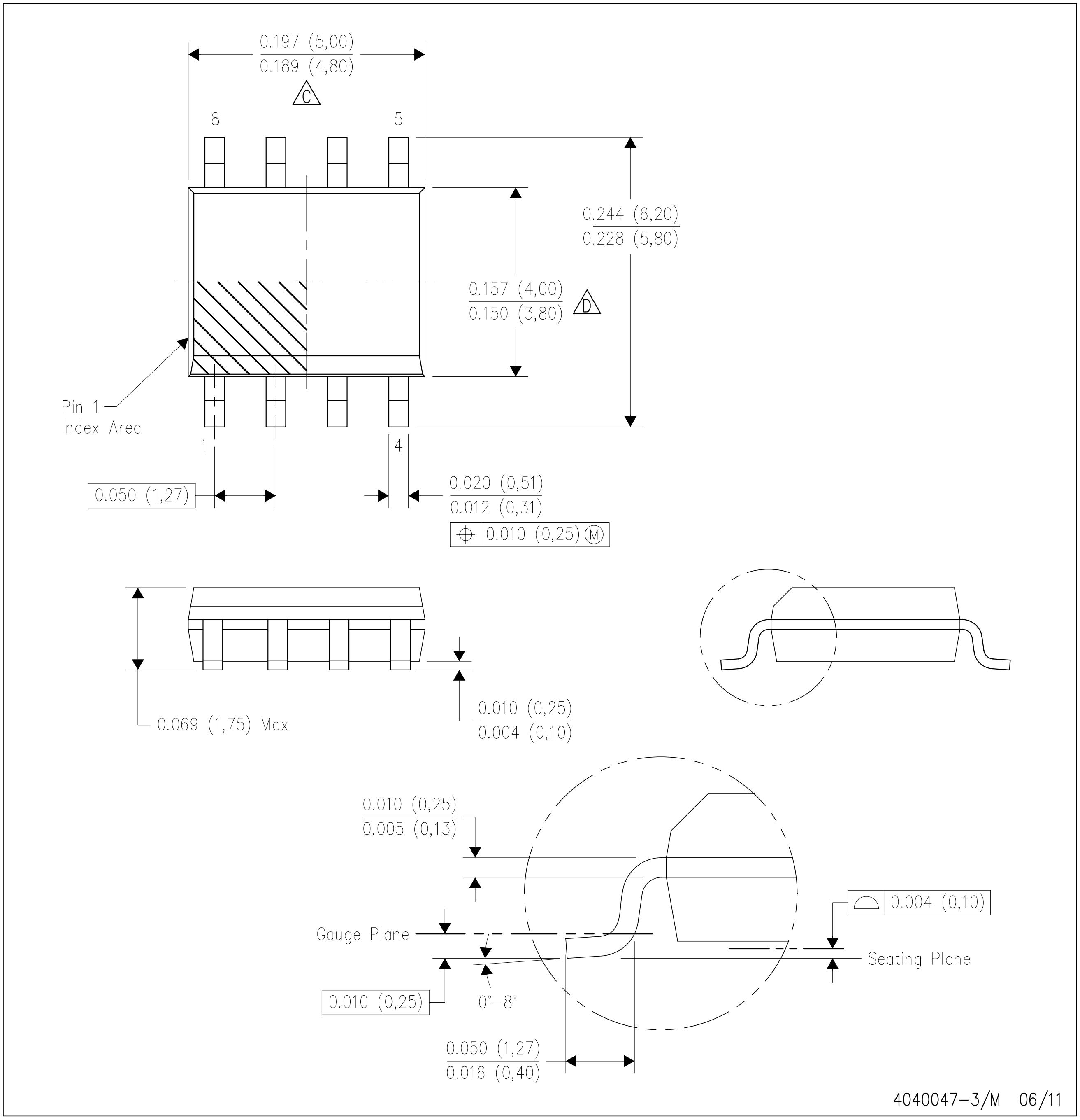
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



4040047–3/M 06/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AA.

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ANALOG
DEVICES

Single and Dual-Supply, Rail-to-Rail, Low Cost Instrumentation Amplifier

Data Sheet

AD623

FEATURES

Easy to use
Rail-to-rail output swing
Input voltage range extends 150 mV below ground (single supply)
Low power, 550 µA maximum supply current
Gain set with one external resistor
  Gain range: 1 to 1000
High accuracy dc performance
  0.10% gain accuracy (G = 1)
  0.35% gain accuracy (G > 1)
Noise: 35 nV/√Hz RTI noise at 1 kHz
Excellent dynamic specifications
  800 kHz bandwidth (G = 1)
  20 µs settling time to 0.01% (G = 10)

APPLICATIONS

Low power medical instrumentation
Transducer interfaces
Thermocouple amplifiers
Industrial process controls
Difference amplifiers
Low power data acquisition

GENERAL DESCRIPTION

The AD623 is an integrated, single- or dual-supply instrumentation amplifier that delivers rail-to-rail output swing using supply voltages from 3 V to 12 V. The AD623 offers superior user flexibility by allowing single gain set resistor programming and by conforming to the 8-lead industry standard pinout configuration. With no external resistor, the AD623 is configured for unity gain (G = 1), and with an external resistor, the AD623 can be programmed for gains of up to 1000.

The superior accuracy of the AD623 is the result of increasing ac common-mode rejection ratio (CMRR) coincident with increasing gain; line noise harmonics are rejected due to constant CMRR up to 200 Hz. The AD623 has a wide input common-mode range and amplifies signals with common-mode voltages as low as 150 mV below ground. The AD623 maintains superior performance with dual and single polarity power supplies.

Table 1. Low Power Upgrades for the AD623

Part No.	Total V_S (V dc)	Typical I_Q (µA)
AD8235	5.5	30
AD8236	5.5	33
AD8237	5.5	33
AD8226	36	350
AD8227	36	325
AD8420	36	85
AD8422	36	300
AD8426	36	325 (per channel)

FUNCTIONAL BLOCK DIAGRAM

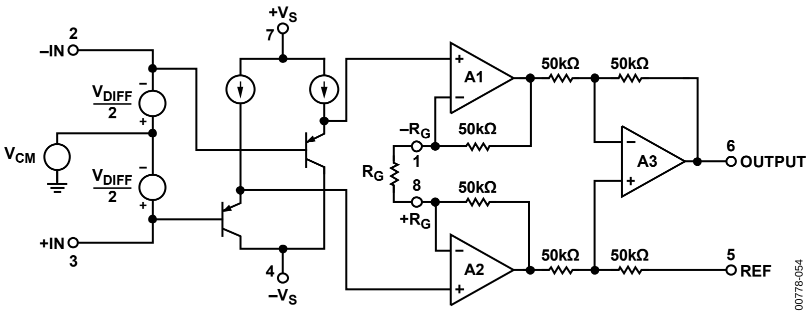

Figure 1.

Rev. E

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Comparable Parts

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Evaluation Kits

- AD62x, AD822x, AD842x Series InAmp Evaluation Board

Documentation

Application Notes

- AN-244: A User's Guide to I.C. Instrumentation Amplifiers
- AN-245: Instrumentation Amplifiers Solve Unusual Design Problems
- AN-282: Fundamentals of Sampled Data Systems
- AN-589: Ways to Optimize the Performance of a Difference Amplifier
- AN-671: Reducing RFI Rectification Errors in In-Amp Circuits

Data Sheet

- AD623: Single Supply, Rail-to-Rail, Low Cost Instrumentation Amplifier Data Sheet

Technical Books

- A Designer's Guide to Instrumentation Amplifiers, 3rd Edition, 2006

User Guides

- UG-261: Evaluation Boards for the AD62x, AD822x and AD842x Series

Tools and Simulations

- In-Amp Error Calculator
- AD623 SPICE Macro-Model

Reference Materials

Technical Articles

- Auto-Zero Amplifiers
- High-performance Adder Uses Instrumentation Amplifiers
- Input Filter Prevents Instrumentation-amp RF-Rectification Errors
- Low Power, Low Cost, Wireless ECG Holter Monitor
- Protecting Instrumentation Amplifiers
- The AD8221 - Setting a New Industry Standard for Instrumentation Amplifiers

Design Resources

- AD623 Material Declaration
- PCN-PDN Information
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SPECIFICATIONS

SINGLE SUPPLY

Typical at 25°C, single supply, $+V_S = 5$ V, $-V_S = 0$ V, and $R_L = 10$ kΩ, unless otherwise noted.

Table 2.

Parameter	Test Conditions/ Comments	AD623A			AD623ARM			AD623B			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GAIN	$G = 1 + (100\ k/R_G)$										
Gain Range		1		1000	1		1000	1		1000	
Gain Error[1]	G1 V_{OUT} = 0.05 V to 3.5 V										
	G > 1 V_{OUT} = 0.05 V to 4.5 V										
G = 1			0.03	0.10		0.03	0.10		0.03	0.05	%
G = 10			0.10	0.35		0.10	0.35		0.10	0.35	%
G = 100			0.10	0.35		0.10	0.35		0.10	0.35	%
G = 1000			0.10	0.35		0.10	0.35		0.10	0.35	%
Nonlinearity	G1 V_{OUT} = 0.05 V to 3.5 V										
	G > 1 V_{OUT} = 0.05 V to 4.5 V										
G = 1 to 1000			50			50			50		ppm
Gain vs. Temperature											
G = 1			5	10		5	10		5	10	ppm/°C
G > 1[1]			50			50			50		ppm/°C
VOLTAGE OFFSET	Total RTI error = $V_{OSI} + V_{OSO}/G$										
Input Offset, V_{OSI}			25	200		200	500		25	100	µV
Over Temperature				350			650			160	µV
Average Temperature Coefficient (Tempco)			0.1	2		0.1	2		0.1	1	µV/°C
Output Offset, V_{OSO}			200	1000		500	2000		200	500	µV
Over Temperature				1500			2600			1100	µV
Average Tempco			2.5	10		2.5	10		2.5	10	µV/°C
Offset Referred to the Input vs. Supply (PSR)											
G = 1		80	100		80	100		80	100		dB
G = 10		100	120		100	120		100	120		dB
G = 100		120	140		120	140		120	140		dB
G = 1000		120	140		120	140		120	140		dB
INPUT CURRENT											
Input Bias Current			17	25		17	25		17	25	nA
Over Temperature				27.5			27.5			27.5	nA
Average Tempco			25			25			25		pA/°C
Input Offset Current			0.25	2		0.25	2		0.25	2	nA
Over Temperature				2.5			2.5			2.5	nA
Average Tempco			5			5			5		pA/°C
INPUT											
Input Impedance											
Differential			2‖2			2‖2			2‖2		GΩ‖pF
Common-Mode			2‖2			2‖2			2‖2		GΩ‖pF
Input Voltage Range[2]	V_S = 3 V to 12 V	$(-V_S) - 0.15$		$(+V_S) - 1.5$	$(-V_S) - 0.15$		$(+V_S) - 1.5$	$(-V_S) - 0.15$		$(+V_S) - 1.5$	V

Parameter	Test Conditions/ Comments	AD623A			AD623ARM			AD623B			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Common-Mode Rejection at 60 Hz with 1 kΩ Source Imbalance											
G = 1	V_{CM} = 0 V to 3 V	70	80		70	80		77	86		dB
G = 10	V_{CM} = 0 V to 3 V	90	100		90	100		94	100		dB
G = 100	V_{CM} = 0 V to 3 V	105	110		105	110		105	110		dB
G = 1000	V_{CM} = 0 V to 3 V	105	110		105	110		105	110		dB
OUTPUT											
Output Swing	R_L = 10 kΩ	0.01		(+V_S) – 0.5	0.01		(+V_S) – 0.5	0.01		(+V_S) – 0.5	V
	R_L = 100 kΩ	0.01		(+V_S) – 0.15	0.01		(+V_S) – 0.15	0.01		(+V_S) – 0.15	V
DYNAMIC RESPONSE											
Small Signal –3 dB BW											
G = 1			800			800			800		kHz
G = 10			100			100			100		kHz
G = 100			10			10			10		kHz
G = 1000			2			2			2		kHz
Slew Rate			0.3			0.3			0.3		V/µs
Settling Time to 0.01%	V_S = 5 V										
G = 1	Step size: 3.5 V		30			30			30		µs
G = 10	Step size: 4 V, V_{CM} = 1.8 V		20			20			20		µs

---

[1] Does not include effects of external resistor, R_G.

[2] One input grounded. G = 1.

DUAL SUPPLIES

Typical at 25°C dual supply, V_S = ±5 V, and R_L = 10 kΩ, unless otherwise noted.

Table 3.

		AD623A			AD623ARM			AD623B			
Parameter	**Test Conditions/ Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
GAIN	G = 1 + (100 k/R_G)										
Gain Range		1		1000	1		1000	1		1000	
Gain Error[1]	G1 V_{OUT} = −4.8 V to +3.5 V G > 1 V_{OUT} = 0.05 V to 4.5 V										
G = 1			0.03	0.10		0.03	0.10		0.03	0.05	%
G = 10			0.10	0.35		0.10	0.35		0.10	0.35	%
G = 100			0.10	0.35		0.10	0.35		0.10	0.35	%
G = 1000			0.10	0.35		0.10	0.35		0.10	0.35	%
Nonlinearity	G1 V_{OUT} = −4.8 V to +3.5 V G > 1 V_{OUT} = −4.8 V to +4.5 V										
G = 1 to 1000			50			50			50		ppm
Gain vs. Temperature											
G = 1			5	10		5	10		5	10	ppm/°C
G > 1[1]			50			50			50		ppm/°C
VOLTAGE OFFSET	Total RTI error = V_{OSI} + V_{OSO}/G										
Input Offset, V_{OSI}			25	200		200	500		25	100	µV
Over Temperature				350			650			160	µV
Average Tempco			0.1	2		0.1	2		0.1	1	µV/°C
Output Offset, V_{OSO}			200	1000		500	2000		200	500	µV
Over Temperature				1500			2600			1100	µV
Average Tempco			2.5	10		2.5	10		2.5	10	µV/°C
Offset Referred to the Input vs. Supply (PSR)											
G = 1		80	100		80	100		80	100		dB
G = 10		100	120		100	120		100	120		dB
G = 100		120	140		120	140		120	140		dB
G = 1000		120	140		120	140		120	140		dB
INPUT CURRENT											
Input Bias Current			17	25		17	25		17	25	nA
Over Temperature				27.5			27.5			27.5	nA
Average Tempco			25			25			25		pA/°C
Input Offset Current			0.25	2		0.25	2		0.25	2	nA
Over Temperature				2.5			2.5			2.5	nA
Average Tempco			5			5			5		pA/°C
INPUT											
Input Impedance											
Differential			2||2			2||2			2||2		GΩ||pF
Common-Mode			2||2			2||2			2||2		GΩ||pF
Input Voltage Range[2]	V_S = +2.5 V to ±6 V	(−V_S) − 0.15		(+V_S) − 1.5	(−V_S) − 0.15		(+V_S) − 1.5	(−V_S) − 0.15		(+V_S) − 1.5	V

Parameter	Test Conditions/ Comments	AD623A Min	AD623A Typ	AD623A Max	AD623ARM Min	AD623ARM Typ	AD623ARM Max	AD623B Min	AD623B Typ	AD623B Max	Unit
Common-Mode Rejection at 60 Hz with 1 kΩ Source Imbalance											
G = 1	V_{CM} = +3.5 V to −5.15 V	70	80		70	80		77	86		dB
G = 10	V_{CM} = +3.5 V to −5.15 V	90	100		90	100		94	100		dB
G = 100	V_{CM} = +3.5 V to −5.15 V	105	110		105	110		105	110		dB
G = 1000	V_{CM} = +3.5 V to −5.15 V	105	110		105	110		105	110		dB
OUTPUT											
Output Swing	R_L = 10 kΩ, V_S = ±5 V	$(-V_S)$ + 0.2		$(+V_S)$ − 0.5	$(-V_S)$ + 0.2		$(+V_S)$ − 0.5	$(-V_S)$ + 0.2		$(+V_S)$ − 0.5	V
	R_L = 100 kΩ	$(-V_S)$ + 0.05		$(+V_S)$ − 0.15	$(-V_S)$ + 0.05		$(+V_S)$ − 0.15	$(-V_S)$ + 0.05		$(+V_S)$ − 0.15	V
DYNAMIC RESPONSE											
Small Signal −3 dB Bandwidth											
G = 1			800			800			800		kHz
G = 10			100			100			100		kHz
G = 100			10			10			10		kHz
G = 1000			2			2			2		kHz
Slew Rate			0.3			0.3			0.3		V/µs
Settling Time to 0.01%	V_S = ±5 V, 5 V step										
G = 1			30			30			30		µs
G = 10			20			20			20		µs

[1] Does not include effects of external resistor, R_G.
[2] One input grounded. G = 1.

SPECIFICATIONS COMMON TO DUAL AND SINGLE SUPPLIES

Table 4.

Parameter	Test Conditions/ Comments	AD623A			AD623ARM			AD623B			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
NOISE											
Voltage Noise, 1 kHz	Total RTI noise = $\sqrt{(e_{ni})^2 + (2e_{no}/G)^2}$										
Input, Voltage Noise, e_{ni}			35			35			35		nV/√Hz
Output, Voltage Noise, e_{no}			50			50			50		nV/√Hz
RTI, 0.1 Hz to 10 Hz											
G = 1			3.0			3.0			3.0		µV p-p
G = 1000			1.5			1.5			1.5		µV p-p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
0.1 Hz to 10 Hz			1.5			1.5			1.5		pA p-p
REFERENCE INPUT											
R_{IN}			100 ± 20%			100 ± 20%			100 ± 20%		kΩ
I_{IN}	$V_{IN}+$, $V_{REF} = 0$ V		50	60		50	60		50	60	µA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Gain to Output			1 ± 0.0002			1 ± 0.0002			1 ± 0.0002		V
POWER SUPPLY											
Operating Range	Dual supply	±2.5		±6	±2.5		±6	±2.5		±6	V
	Single supply	2.7		12	2.7		12	2.7		12	V
Quiescent Current	Dual supply		375	550		375	550		375	550	µA
	Single supply		305	480		305	480		305	480	µA
Over Temperature				625			625			625	µA
TEMPERATURE RANGE											
For Specified Performance		−40		+85	−40		+85	−40		+85	°C

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	12 V
Internal Power Dissipation[1]	650 mW
Differential Input Voltage	±6 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] Specification is for device in free air:
8-Lead PDIP Package: θ_{JA} = 95°C/W
8-Lead SOIC Package: θ_{JA} = 155°C/W
8-Lead MSOP Package: θ_{JA} = 200°C/W

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

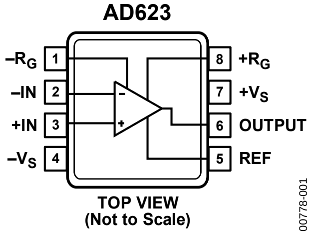


Figure 2. AD623 Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$-R_G$	Inverting Terminal of External Gain-Setting Resistor, R_G.
2	−IN	Inverting In-Amp Input.
3	+IN	Noninverting In-Amp Input.
4	$-V_S$	Negative Supply Terminal.
5	REF	In-Amp Output Reference Input. The voltage input establishes the common-mode voltage of the output.
6	OUTPUT	In-Amp Output.
7	$+V_S$	Positive Supply Terminal.
8	$+R_G$	Noninverting Terminal of External Gain Setting Resistor, R_G.

TYPICAL PERFORMANCE CHARACTERISTICS

At 25°C, $V_S = \pm 5$ V, and $R_L = 10$ kΩ, unless otherwise noted.

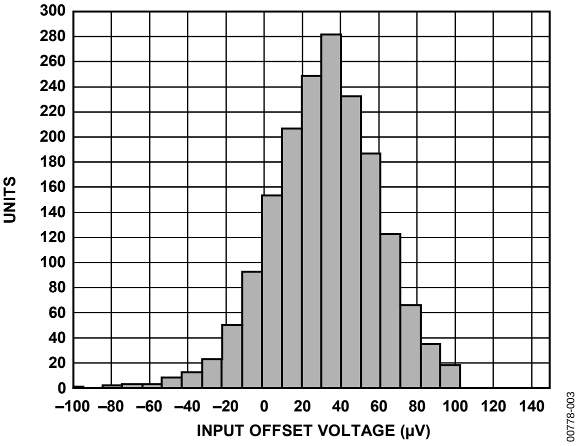


Figure 3. Typical Distribution of Input Offset Voltage, N-8 and R-8 Package Options

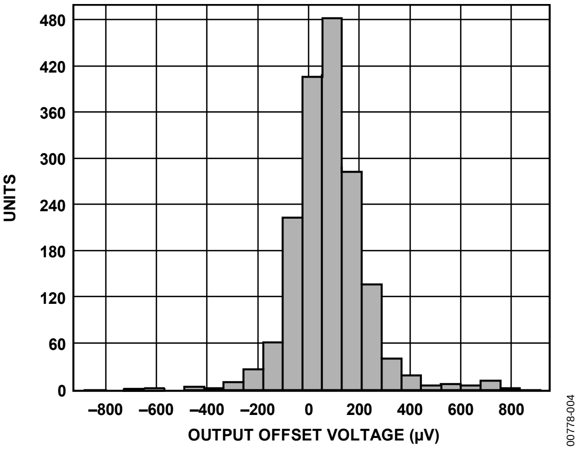


Figure 4. Typical Distribution of Output Offset Voltage, N-8 and R-8 Package Options

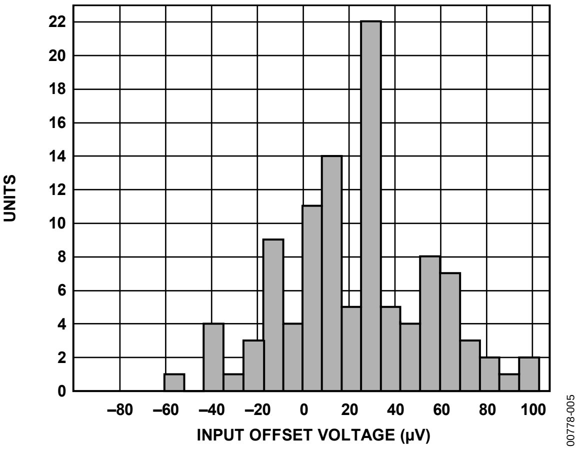


Figure 5. Typical Distribution of Input Offset Voltage, $+V_S = 5$ V, $-V_S = 0$ V, $V_{REF} = -0.125$ V, N-8 and R-8 Package Options

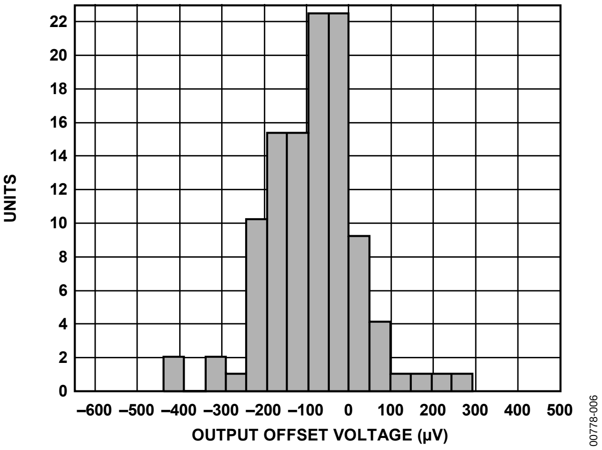


Figure 6. Typical Distribution of Output Offset Voltage, $+V_S = 5$ V, $-V_S = 0$ V, $V_{REF} = -0.125$ V, N-8 and R-8 Package Options

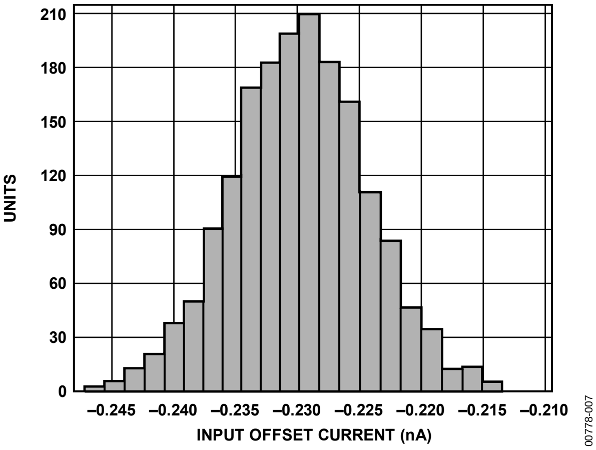


Figure 7. Typical Distribution for Input Offset Current, N-8 and R-8 Package Options

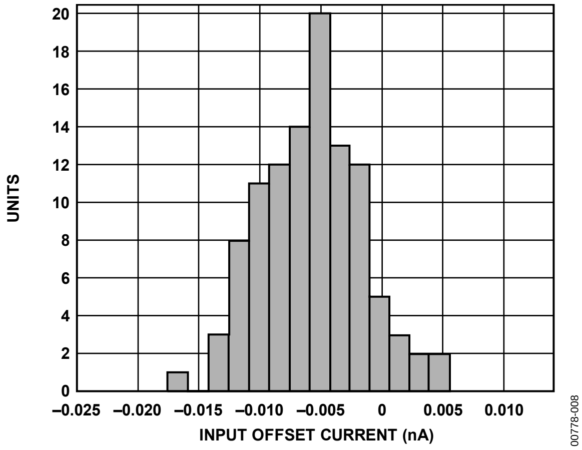


Figure 8. Typical Distribution for Input Offset Current, $+V_S = 5$ V, $-V_S = 0$ V, $V_{REF} = -0.125$ V, N-8 and R-8 Package Options

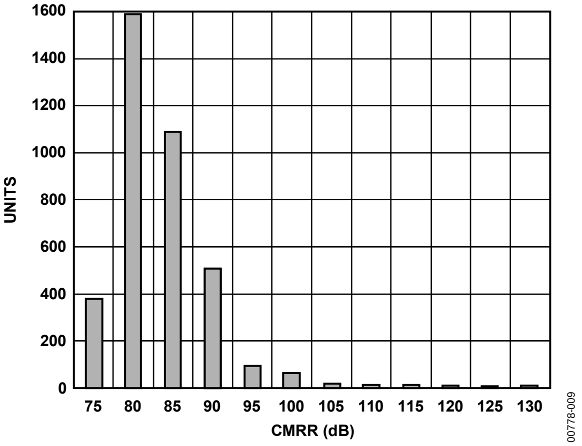


Figure 9. Typical Distribution for CMRR (G = 1)

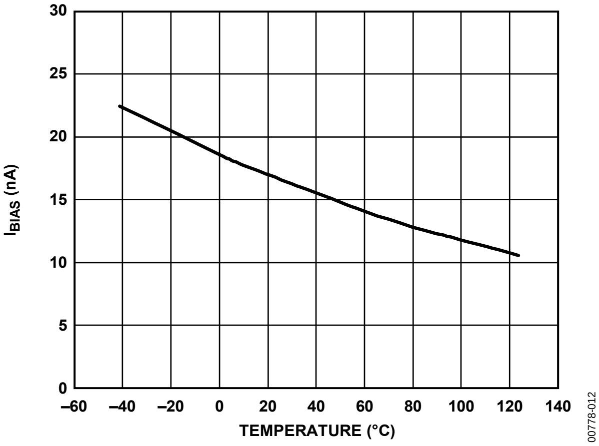


Figure 12. I_{BIAS} vs. Temperature

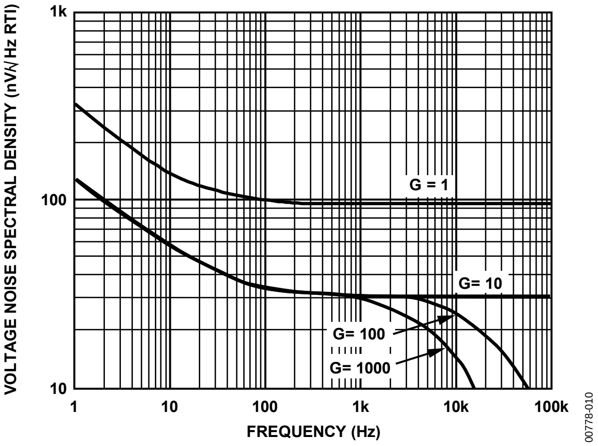


Figure 10. Voltage Noise Spectral Density vs. Frequency

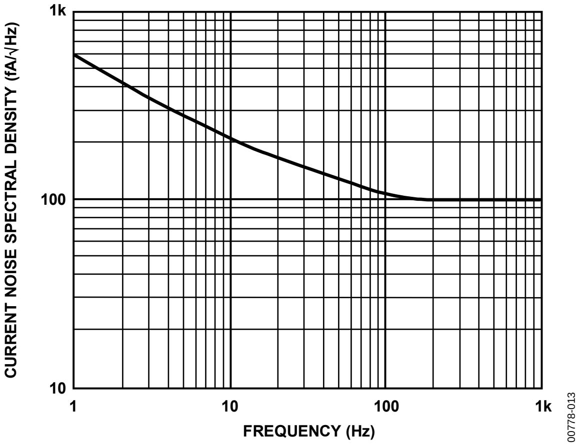


Figure 13. Current Noise Spectral Density vs. Frequency

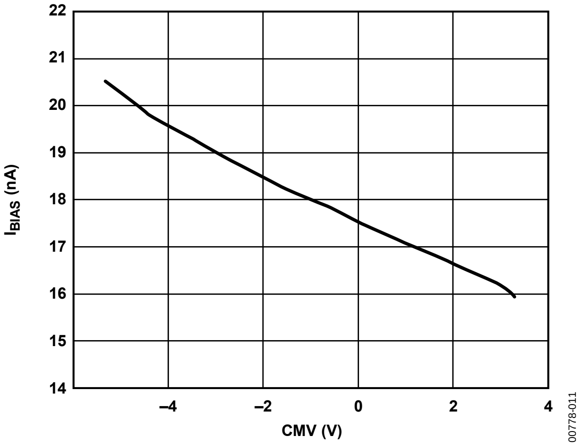


Figure 11. I_{BIAS} vs. CMV

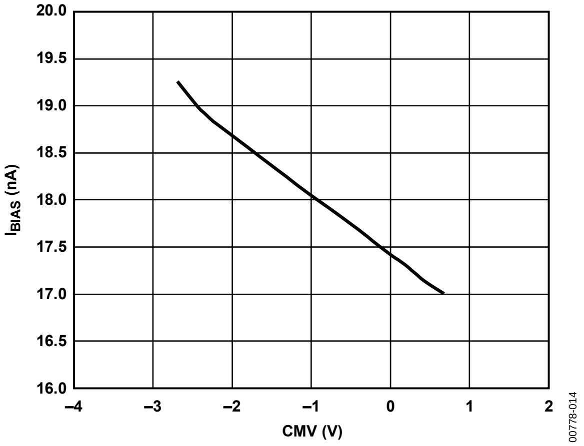


Figure 14. I_{BIAS} vs. CMV, V_S = ±2.5 V

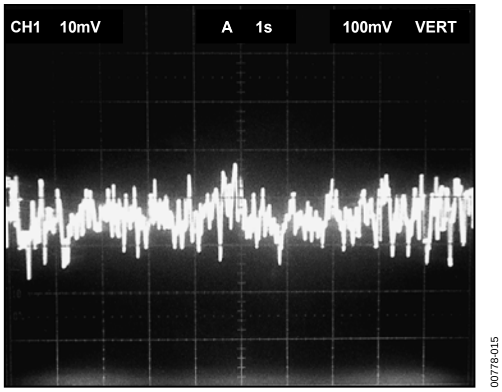


Figure 15. 0.1 Hz to 10 Hz Current Noise (0.71 pA/DIV)

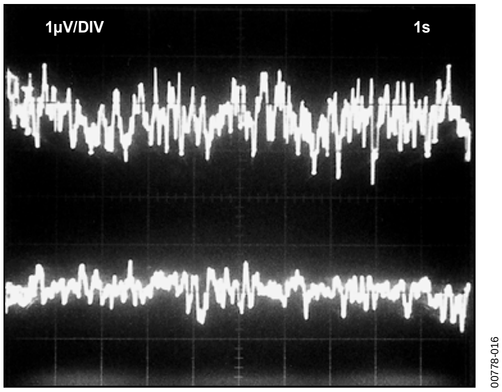


Figure 16. 0.1 Hz to 10 Hz RTI Voltage Noise (1 DIV = 1 µV p-p)

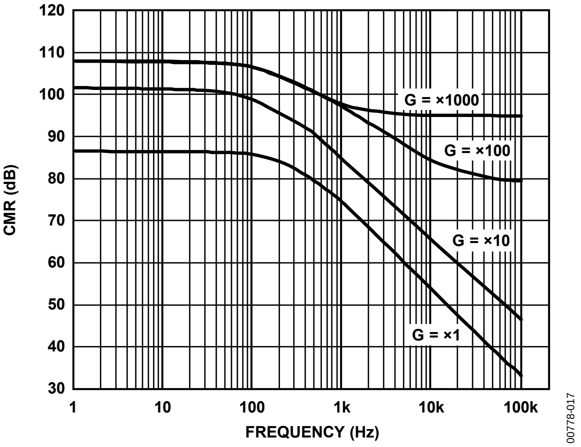


Figure 17. Common-Mode Rejection (CMR) vs. Frequency, $+V_S = 5$ V, $-V_S = 0$ V, $V_{REF} = 2.5$ V, for Various Gain Settings (G)

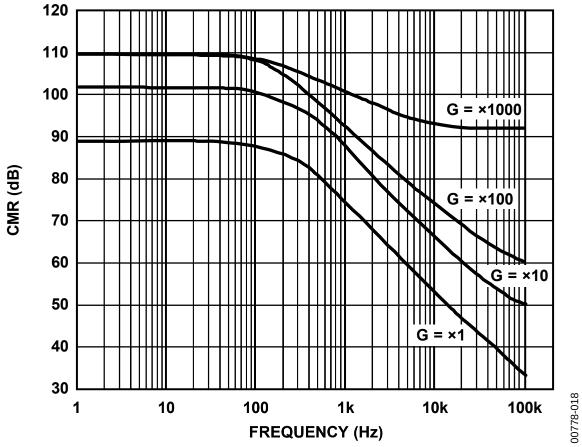


Figure 18. CMR vs. Frequency for Various Gain Settings (G)

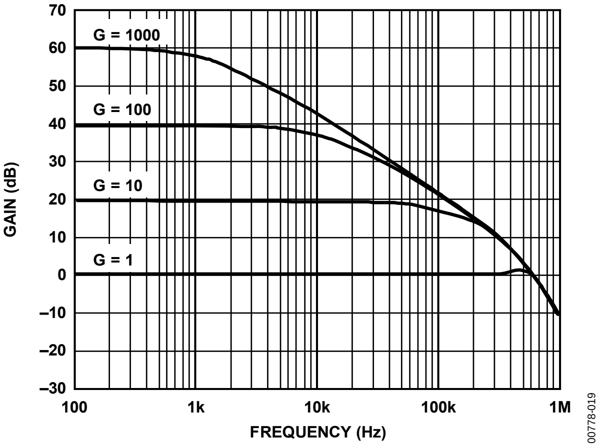


Figure 19. Gain vs. Frequency ($+V_S = 5$ V, $-V_S = 0$ V), $V_{REF} = 2.5$ V, for Various Gain Settings (G)

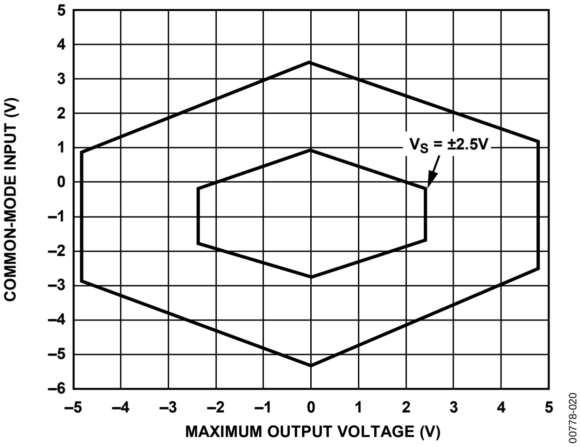


Figure 20. Maximum Output Voltage vs. Common-Mode Input, G = 1, $R_L = 100$ kΩ for Two Supply Voltages

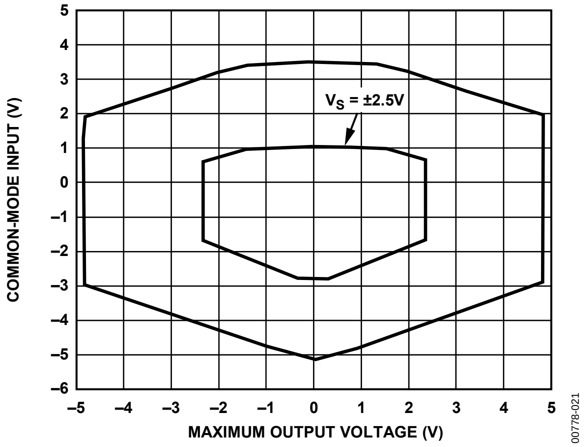


Figure 21. Maximum Output Voltage vs. Common-Mode Input, G ≥ 10, R_L = 100 Ω, for Two Supply Voltages

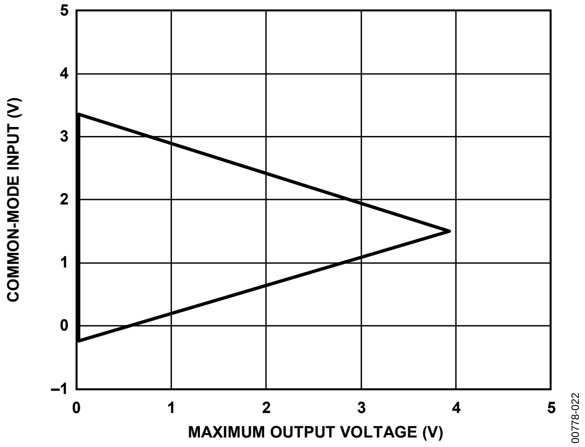


Figure 22. Maximum Output Voltage vs. Common-Mode Input, G = 1, +V_S = 5 V, −V_S = 0 V, R_L = 100 kΩ

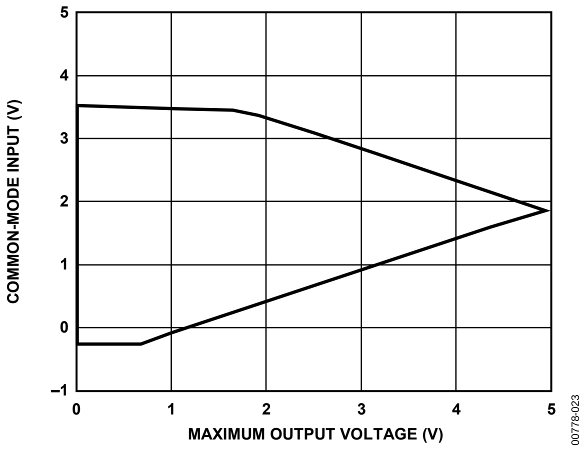


Figure 23. Maximum Output Voltage vs. Common-Mode Input, G ≥ 10, +V_S = 5 V, −V_S = 0 V, R_L = 100 kΩ

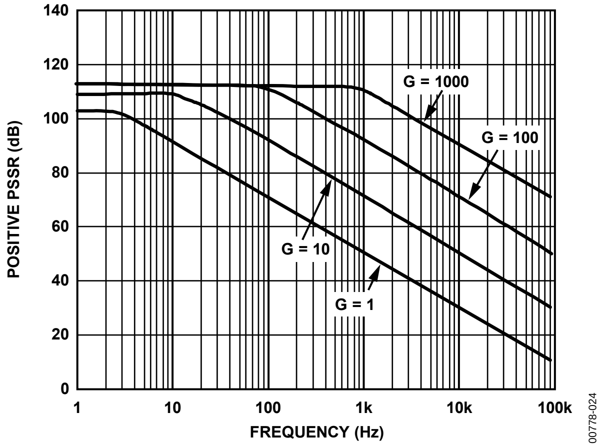


Figure 24. Positive PSRR vs. Frequency

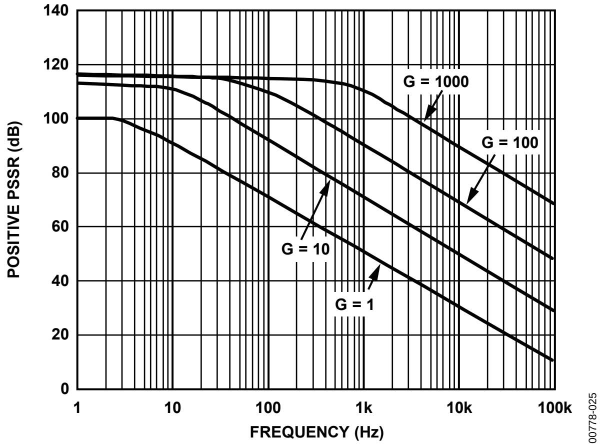


Figure 25. Positive PSRR vs. Frequency, +V_S = 5V, −V_S = 0 V, for Various Gain Settings (G)

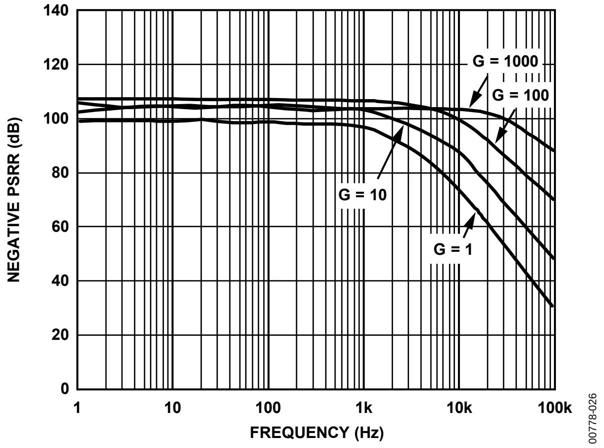


Figure 26. Negative PSRR vs. Frequency for Various Gain Settings (G)

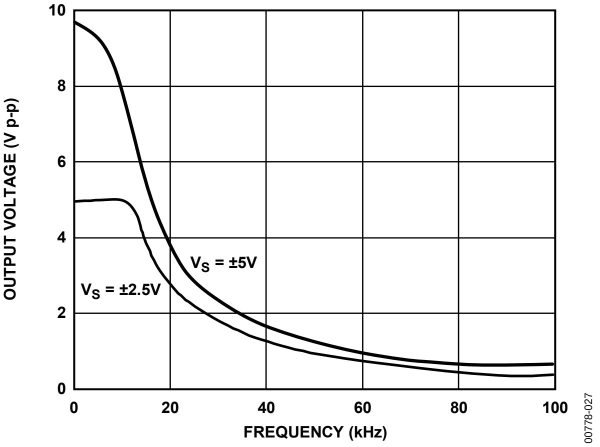


Figure 27. Large Signal Response, G ≤ 10 for Two Supply Voltages

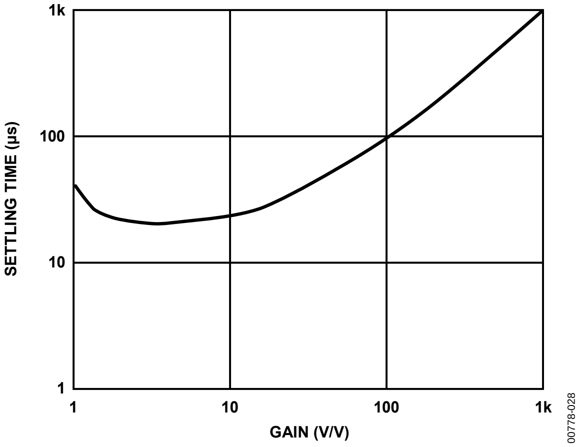


Figure 28. Settling Time to 0.01% vs. Gain, for a 5 V Step at Output, C_L = 100 pF

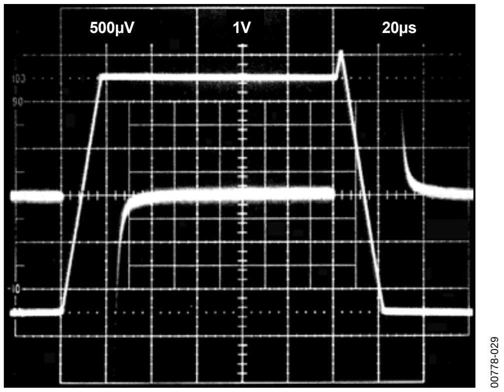


Figure 29. Large Signal Pulse Response and Settling Time, G = −1 (0.250 mV = 0.01%), C_L = 100 pF

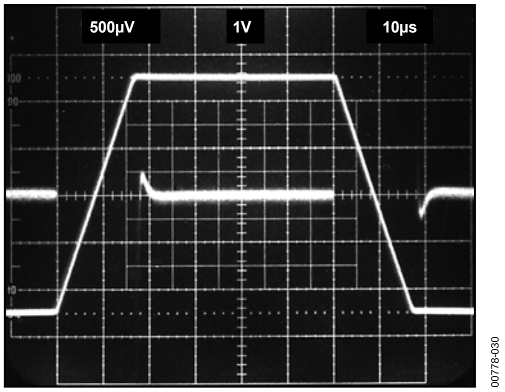


Figure 30. Large Signal Pulse Response and Settling Time, G = −10 (0.250 mV = 0.01%), C_L = 100 pF

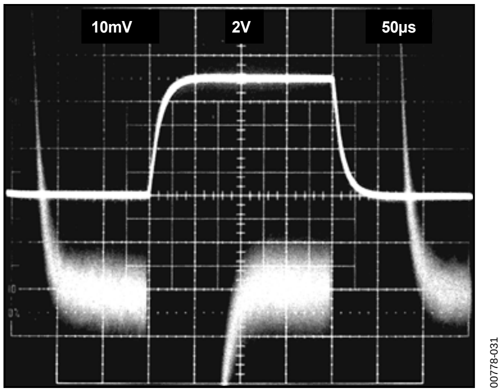


Figure 31. Large Signal Pulse Response and Settling Time, G = 100, C_L = 100 pF

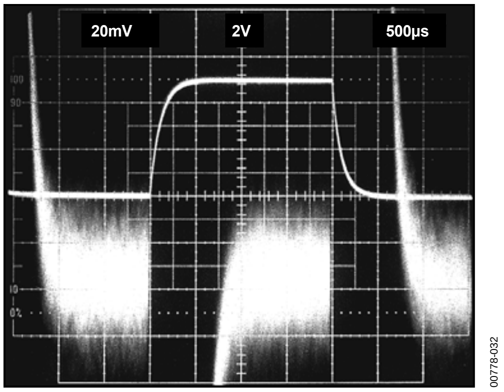


Figure 32. Large Signal Pulse Response and Settling Time, G = −1000 (5 mV = 0.01%), C_L = 100 pF

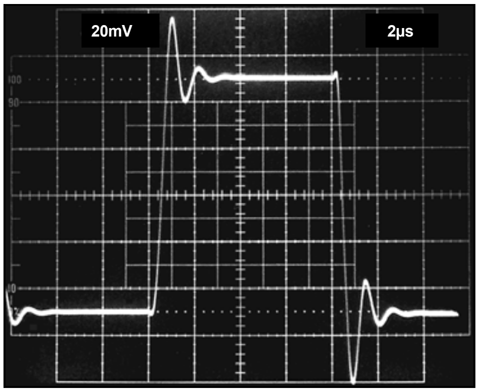


Figure 33. Small Signal Pulse Response, G = 1, R_L = 10 kΩ, C_L = 100 pF

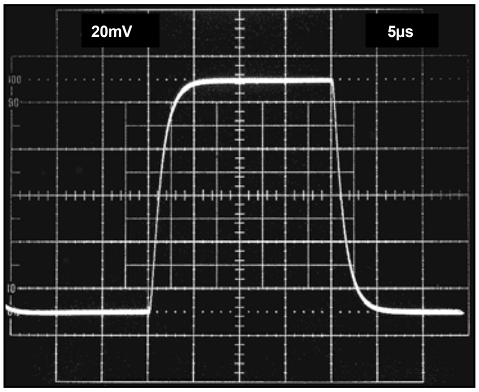


Figure 34. Small Signal Pulse Response, G = 10, R_L = 10 kΩ, C_L = 100 pF

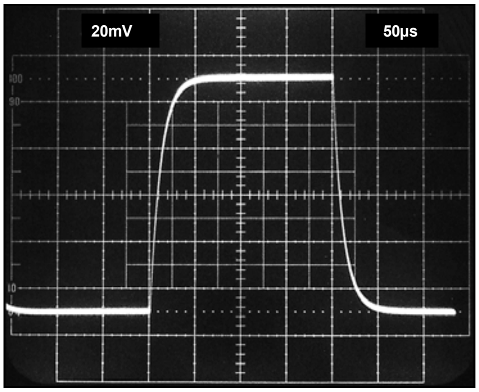


Figure 35. Small Signal Pulse Response, G = 100, R_L = 10 kΩ, C_L = 100 pF

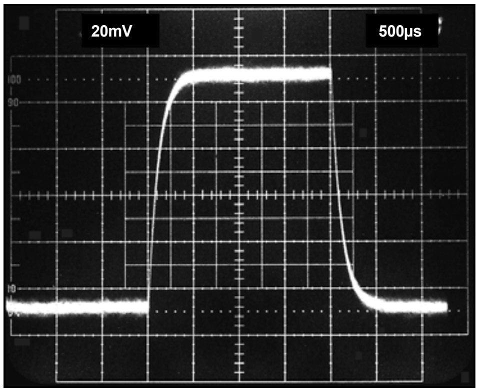


Figure 36. Small Signal Pulse Response, G = 1000, R_L = 10 kΩ, C_L = 100 pF

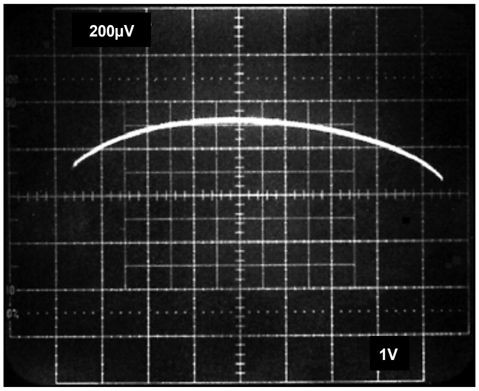


Figure 37. Gain Nonlinearity, G = −1 (50 ppm/DIV)

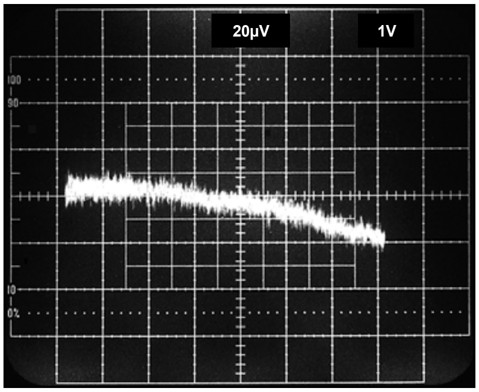


Figure 38. Gain Nonlinearity, G = −10 (6 ppm/DIV)

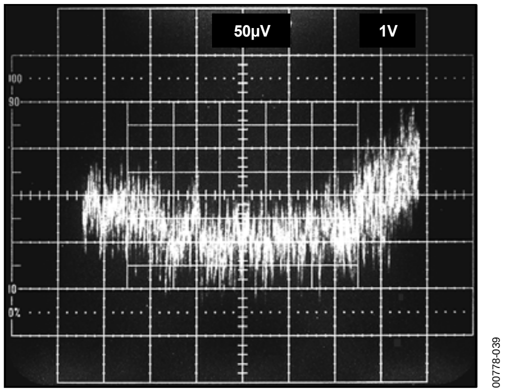


Figure 39. Gain Nonlinearity, G = −100, 15 ppm/DIV

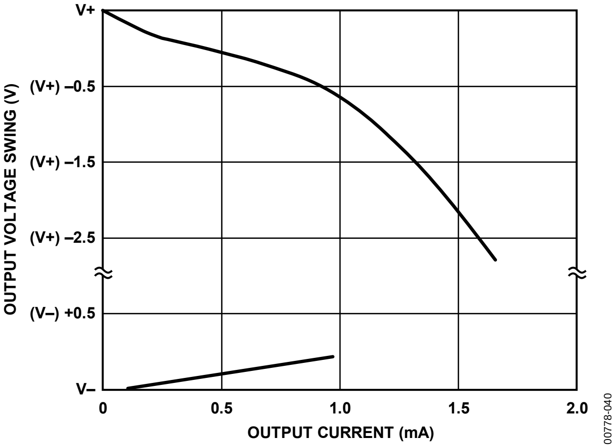


Figure 40. Output Voltage Swing vs. Output Current

THEORY OF OPERATION

The AD623 is an instrumentation amplifier based on a modified classic 3-op-amp approach, to assure single- or dual-supply operation even at common-mode voltages at the negative supply rail. Low voltage offsets, input and output, as well as absolute gain accuracy, and one external resistor to set the gain, make the AD623 one of the most versatile instrumentation amplifiers in its class.

The input signal is applied to PNP transistors acting as voltage buffers and providing a common-mode signal to the input amplifiers (see Figure 41). An absolute value 50 kΩ resistor in each amplifier feedback assures gain programmability.

The differential output is

$$V_O = \left(1 + \frac{100\ \text{k}\Omega}{R_G}\right) V_C$$

The differential voltage is then converted to a single-ended voltage using the output amplifier, which also rejects any common-mode signal at the output of the input amplifiers.

Because the amplifiers can swing to either supply rail, as well as have their common-mode range extended to below the negative supply rail, the range over which the AD623 can operate is further enhanced (see Figure 20 and Figure 21).

The output voltage at Pin 6 is measured with respect to the potential at Pin 5. The impedance of the reference pin is 100 kΩ; therefore, in applications requiring voltage conversion, a small resistor between Pin 5 and Pin 6 is all that is needed.

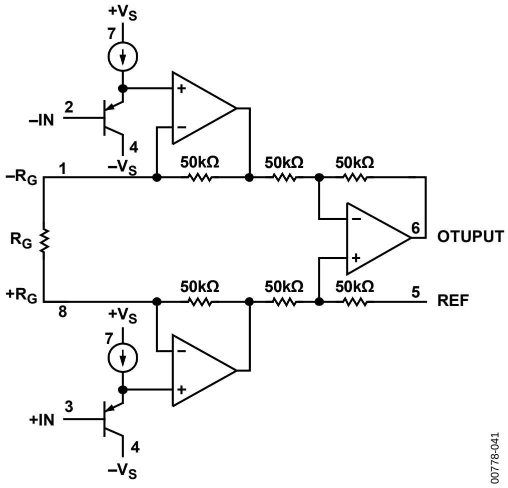


Figure 41. Simplified Schematic

Because of the voltage feedback topology of the internal op amps, the bandwidth of the in-amp decreases with increasing gain. At unity gain, the output amplifier limits the bandwidth.

APPLICATIONS INFORMATION

BASIC CONNECTION

Figure 42 and Figure 43 show the basic connection circuits for the AD623. The $+V_S$ and $-V_S$ terminals are connected to the power supply. The supply can be either bipolar ($V_S = \pm 2.5$ V to ± 6 V) or single supply ($-V_S = 0$ V, $+V_S = 3.0$ V to 12 V). Capacitively decouple power supplies close to the power pins of the device. For best results, use surface-mount 0.1 µF ceramic chip capacitors and 10 µF electrolytic tantalum capacitors.

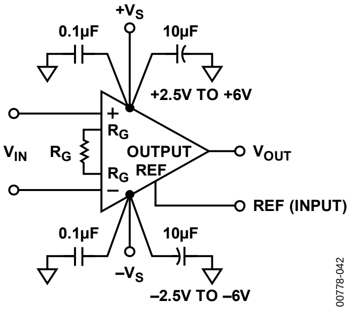


Figure 42. Dual-Supply Basic Connection

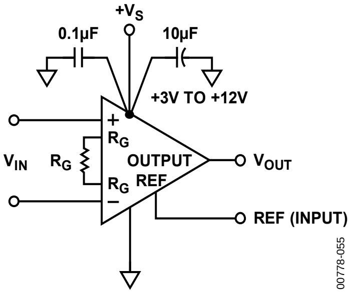


Figure 43. Single-Supply Basic Connection

The input voltage, which can be either single-ended (tie either −IN or +IN to ground) or differential, is amplified by the programmed gain. The output signal appears as the voltage difference between the OUTPUT pin and the externally applied voltage on the REF input. For a ground referenced output, REF must be grounded.

GAIN SELECTION

The gain of the AD623 is programmed by the R_G resistor, or more precisely, by whatever impedance appears between Pin 1 and Pin 8. The AD623 offers accurate gains using 0.1% to 1% tolerance resistors. Table 7 shows the required values of R_G for the various gains. Note that for G = 1, the R_G terminals are unconnected ($R_G = \infty$). For any arbitrary gain, R_G can be calculated by

$$R_G = 100\ \text{k}\Omega/(G - 1)$$

REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output. The reference terminal is also useful when bipolar signals are being amplified because it can be used to provide a virtual ground voltage. The voltage on the reference terminal can be varied from $-V_S$ to $+V_S$.

Table 7. Required Values of Gain Resistors

Desired Gain	1% Standard Table Value of R_G	Calculated Gain Using 1% Resistors
2	100 kΩ	2
5	24.9 kΩ	5.02
10	11 kΩ	10.09
20	5.23 kΩ	20.12
33	3.09 kΩ	33.36
40	2.55 kΩ	40.21
50	2.05 kΩ	49.78
65	1.58 kΩ	64.29
100	1.02 kΩ	99.04
200	499 Ω	201.4
500	200 Ω	501
1000	100 Ω	1001

INPUT AND OUTPUT OFFSET VOLTAGE ERROR

The offset voltage (V_{OS}) of the AD623 is attributed to two sources: those originating in the two input stages where the in-amp gain is established, and those originating in the subtractor output stage. The output error is divided by the programmed gain when referred to the input. In practice, the input errors dominate at high gain settings, whereas the output error prevails when the gain is set at or near unity.

The V_{OS} error for any given gain is calculated as follows:

$$\text{Total Error Referred to Input (RTI)} = \text{Input Error} + (\text{Output Error}/G)$$

$$\text{Total Error Referred to Output (RTO)} = (\text{Input Error} \times G) + \text{Output Error}$$

The RTI offset errors and noise voltages for different gains are listed in Table 8.

INPUT PROTECTION

Internal supply-referenced clamping diodes allow the input, reference, output, and gain terminals of the AD623 to safely withstand overvoltages of 0.3 V above or below the supplies. This overvoltage protection is true at all gain settings and when cycling power on and off. Overvoltage protection is particularly important because the signal source and amplifier may be powered separately.

If the overvoltage is expected to exceed this value, the current through these diodes must be limited to about 10 mA using external current limiting resistors (see Figure 44). The size of this resistor is defined by the supply voltage and the required overvoltage protection.

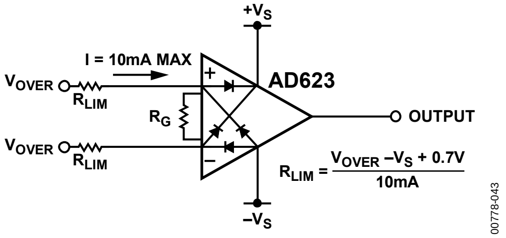
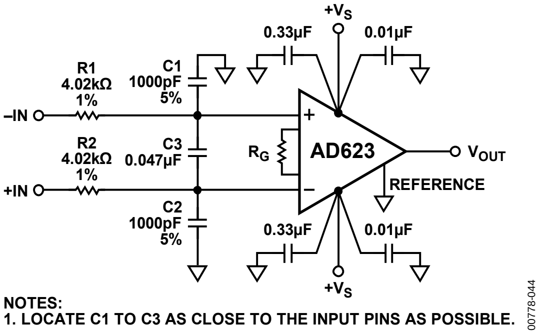


Figure 44. Input Protection

RF INTERFERENCE

All instrumentation amplifiers can rectify high frequency out-of-band signals. Once rectified, these signals appear as dc offset errors at the output. The circuit in Figure 45 provides good RFI suppression without reducing performance within the pass band of the in-amp. Resistor R1 and Capacitor C1 (and likewise, R2 and C2) form a low-pass RC filter that has a −3 dB bandwidth equal to $f = 1/(2\,\pi\,R1C1)$. Using the component values shown, this filter has a −3 dB bandwidth of approximately 40 kHz. The R1 and R2 resistors were selected to be large enough to isolate the input of the circuit from the capacitors, but not large enough to significantly increase the noise of the circuit. To preserve common-mode rejection in the pass band of the amplifier, the C1 and C2 capacitors must be 5% or better units, or low cost 20% units can be tested and binned to provide closely matched devices.



NOTES:
1. LOCATE C1 TO C3 AS CLOSE TO THE INPUT PINS AS POSSIBLE.

Figure 45. Circuit to Attenuate RF Interference

Capacitor C3 is needed to maintain common-mode rejection at low frequencies. R1/R2 and C1/C2 form a bridge circuit whose output appears across the input pins of the in-amp. Any mismatch between C1 and C2 unbalances the bridge and reduces the common-mode rejection. C3 ensures that any RF signals are common mode (the same on both in-amp inputs) and are not applied differentially. This second low-pass network, R1 + R2 and C3, has a −3 dB frequency equal to $1/(2\pi(R1 + R2)(C3))$. Using a C3 value of 0.047 µF, the −3 dB signal bandwidth of this circuit is approximately 400 Hz. The typical dc offset shift over frequency is less than 1.5 µV, and the RF signal rejection of the circuit is better than 71 dB. The 3 dB signal bandwidth of this circuit can be increased to 900 Hz by reducing R1 and R2 to 2.2 kΩ. The performance is similar to using 4 kΩ resistors, except that the circuitry preceding the in-amp must drive a lower impedance load.

Table 8. RTI Error Sources

	Maximum Total Input Offset Error (µV)		Maximum Total Input Offset Drift (µV/°C)		Total Input Referred Noise (nV/√Hz)	
Gain	**AD623A**	**AD623B**	**AD623A**	**AD623B**	**AD623A**	**AD623B**
1	1200	600	12	11	62	62
2	700	350	7	6	45	45
5	400	200	4	3	38	38
10	300	150	3	2	35	35
20	250	125	2.5	1.5	35	35
50	220	110	2.2	1.2	35	35
100	210	105	2.1	1.1	35	35
1000	200	100	2	1	35	35

The circuit in Figure 45 must be built using a printed circuit board (PCB) with a ground plane on both sides. All component leads must be as short as possible. The R1 and R2 resistors can be common 1% metal film units; however, the C1 and C2 capacitors must be ±5% tolerance devices to avoid degrading the common-mode rejection of the circuit. Either the traditional 5% silver mica units or Panasonic ±2% PPS film capacitors are recommended.

In many applications, shielded cables are used to minimize noise; for best CMR over frequency, the shield must be properly driven. Figure 46 shows an active guard driver that is configured to improve ac common-mode rejection by bootstrapping the capacitances of input cable shields, thus minimizing the capacitance mismatch between the inputs.

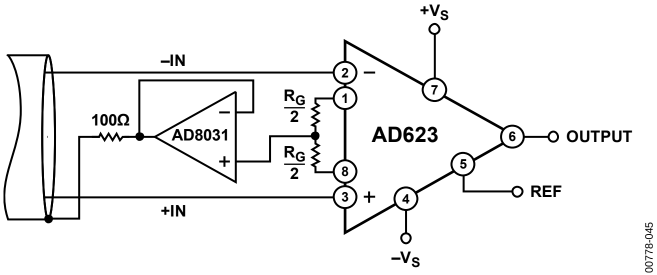


Figure 46. Common-Mode Shield Driver

GROUNDING

Because the AD623 output voltage is developed with respect to the potential on the reference terminal, many grounding problems can be solved by simply tying the REF pin to the appropriate local ground. The REF pin must, however, be tied to a low impedance point for optimal CMR.

The use of ground planes is recommended to minimize the impedance of ground returns (and hence the size of dc errors). To isolate low level analog signals from a noisy digital environment, many data acquisition components have separate analog and digital ground returns (see Figure 47). All ground pins from mixed signal components, such as analog-to-digital converters (ADCs), must be returned through the high quality analog ground plane. Maximum isolation between analog and digital is achieved by connecting the ground planes back at the supplies. The digital return currents from the ADC that flow in the analog ground plane, in general, have a negligible effect on noise performance.

If there is only a single power supply available, it must be shared by both digital and analog circuitry. Figure 48 shows how to minimize interference between the digital and analog circuitry. As in the previous case, use separate analog and digital ground planes (reasonably thick traces can be used as an alternative to a digital ground plane). These ground planes must be connected at the ground pin of the power supply. Run separate traces from the power supply to the supply pins of the digital and analog circuits. Ideally, each device has its own power supply trace, but these can be shared by a number of devices, as long as a single trace is not used to route current to both digital and analog circuitry.

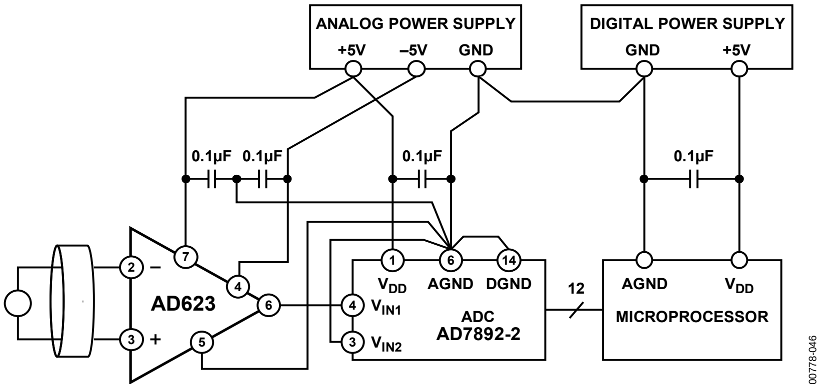


Figure 47. Optimal Grounding Practice for a Bipolar Supply Environment with Separate Analog and Digital Supplies

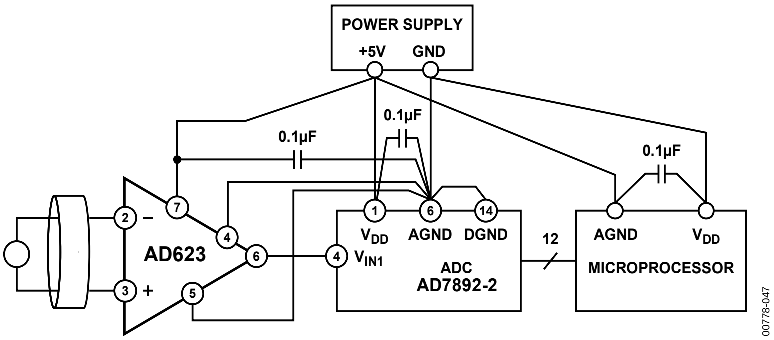


Figure 48. Optimal Ground Practice in a Single-Supply Environment

Ground Returns for Input Bias Currents

Input bias currents are those dc currents that must flow to bias the input transistors of an amplifier. These are usually transistor base currents. When amplifying floating input sources, such as transformers or ac-coupled sources, there must be a direct dc path into each input so that the bias current can flow. Figure 49, Figure 50, and Figure 51 show how a bias current path can be provided for the cases of transformer coupling, thermocouple, and capacitive ac coupling. In dc-coupled resistive bridge applications, providing this path is generally not necessary because the bias current simply flows from the bridge supply through the bridge into the amplifier. However, if the impedances that the two inputs see are large and differ by a large amount (>10 kΩ), the offset current of the input stage causes dc errors proportional with the input offset voltage of the amplifier.

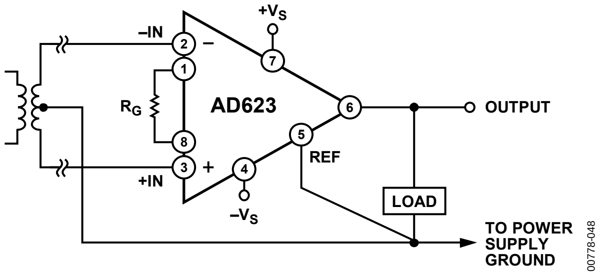


Figure 49. Ground Returns for Bias Currents with Transformer-Coupled Inputs

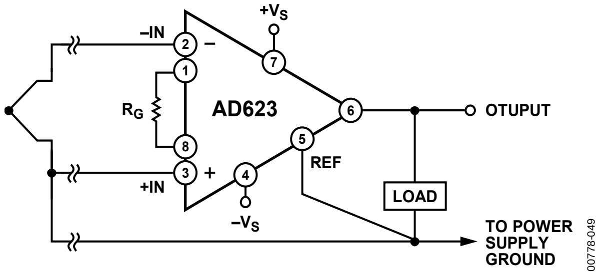


Figure 50. Ground Returns for Bias Currents with Thermocouple Inputs

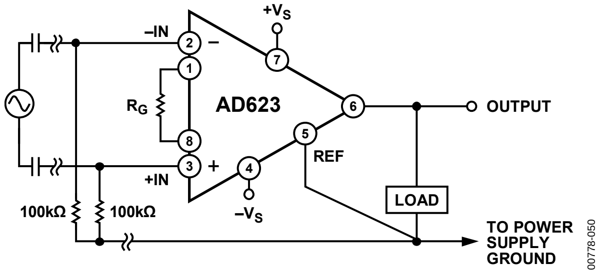


Figure 51. Ground Returns for Bias Currents with AC-Coupled Inputs

Output Buffering

The AD623 is designed to drive loads of 10 kΩ or greater. If the load is less than this value, the output of the AD623 must be buffered with a precision single-supply op amp, such as the OP113. This op amp can swing from 0 V to 4 V on its output while driving a load as small as 600 Ω. Table 9 summarizes the performance of some buffer op amps.

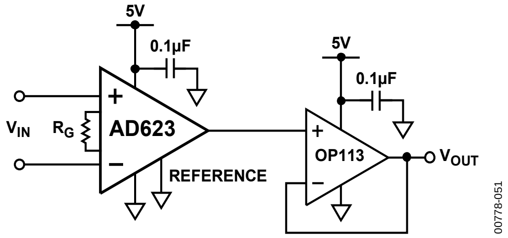


Figure 52. Output Buffering

Table 9. Buffering Options

Op Amp	Description
OP113	Single-supply, high output current
OP191	Rail-to-rail input and output, low supply current

Single-Supply Data Acquisition System

Interfacing bipolar signals to single-supply ADCs presents a challenge. The bipolar signal must be mapped into the input range of the ADC. Figure 53 shows how this translation can be achieved.

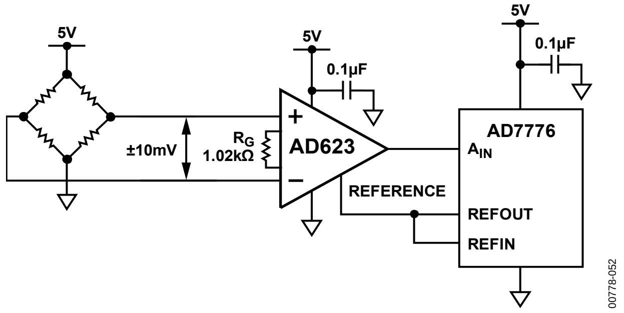


Figure 53. A Single-Supply Data Acquisition System

The bridge circuit is excited by a 5 V supply. The full-scale output voltage from the bridge (±10 mV) therefore has a common-mode level of 2.5 V. The AD623 removes the common-mode component and amplifies the input signal by a factor of 100 (R_{GAIN} = 1.02 kΩ), which results in an output signal of ±1 V. To prevent this signal from running into the ground rail of the AD623, the voltage on the REF pin must be raised to at least 1 V. In this example, the 2 V reference voltage from the AD7776 ADC biases the output voltage of the AD623 to 2 V ± 1 V, which corresponds to the input range of the ADC.

Amplifying Signals with Low Common-Mode Voltage

Because the common-mode input range of the AD623 extends 0.1 V below ground, it is possible to measure small differential signals which have low or no common-mode component. Figure 54 shows a thermocouple application where one side of the J-type thermocouple is grounded.

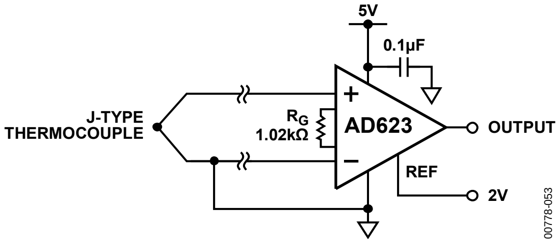


Figure 54. Amplifying Bipolar Signals with Low Common-Mode Voltage

Over a temperature range of −200°C to +200°C, the J-type thermocouple delivers a voltage ranging from −7.890 mV to +10.777 mV. A programmed gain on the AD623 of 100 (R_G = 1.02 kΩ) and a voltage on the REF pin of 2 V result in the output voltage ranging from 1.110 V to 3.077 V relative to ground.

INPUT DIFFERENTIAL AND COMMON-MODE RANGE vs. SUPPLY AND GAIN

Figure 55 shows a simplified block diagram of the AD623. The voltages at the outputs of Amplifier A1 and Amplifier A2 are given by

$$V_{A2} = V_{CM} + V_{DIFF}/2 + 0.6\ V + V_{DIFF} \times R_F/R_G$$
$$= V_{CM} + 0.6\ V + V_{DIFF} \times Gain/2$$

$$V_{A1} = V_{CM} - V_{DIFF}/2 + 0.6\ V + V_{DIFF} \times R_F/R_G$$
$$= V_{CM} + 0.6\ V - V_{DIFF} \times Gain/2$$

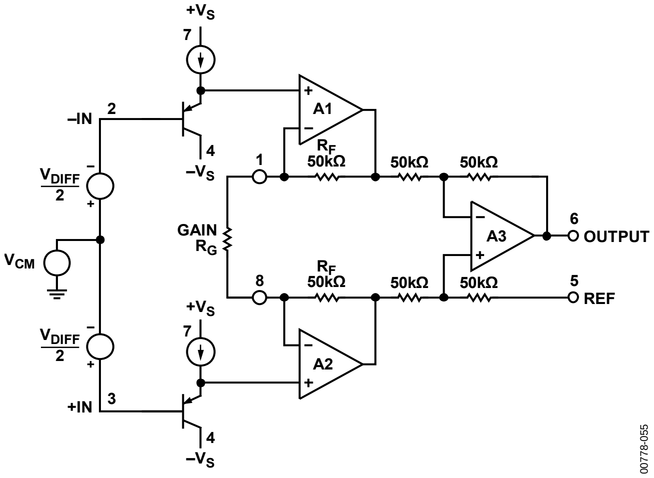


Figure 55. Simplified Block Diagram

The voltages on these internal nodes are critical in determining whether the output voltage is clipped. The V_{A1} and V_{A2} voltages can swing from approximately 10 mV above the negative supply (V− or ground) to within approximately 100 mV of the positive rail before clipping occurs. Based on this and from the previous equations, the maximum and minimum input common-mode voltages are given by the following equations:

$$V_{CMMAX} = V+ - 0.7\ V - V_{DIFF} \times Gain/2$$

$$V_{CMMIN} = V- - 0.590\ V + V_{DIFF} \times Gain/2$$

These equations can be rearranged to give the maximum possible differential voltage (positive or negative) for a particular common-mode voltage, gain, and power supply. Because the signals on A1 and A2 can clip on either rail, the maximum differential voltage is the lesser of the two equations.

$$|V_{DIFFMAX}| = 2\ (V+ - 0.7\ V - V_{CM})/Gain$$

$$|V_{DIFFMAX}| = 2\ (V_{CM} - V- +0.590\ V)/Gain$$

However, the range on the differential input voltage range is also constrained by the output swing. Therefore, the range of V_{DIFF} may need to be lower according the following equation:

$$Input\ Range \leq Available\ Output\ Swing/Gain$$

For a bipolar input voltage with a common-mode voltage that is roughly half way between the rails, $V_{DIFFMAX}$ is half the value that the previous equations yield because the REF pin is at midsupply. Note that the available output swing is given for different supply conditions in the Specifications section.

The equations can be rearranged to give the maximum gain for a fixed set of input conditions. The maximum gain is the lesser of the two equations.

$$Gain_{MAX} = 2\ (V+ - 0.7\ V - V_{CM})/V_{DIFF}$$

$$Gain_{MAX} = 2\ (V_{CM} - V- +0.590\ V)/V_{DIFF}$$

Again, it is recommended that the resulting gain times the input range is less than the available output swing. If this is not the case, the maximum gain is given by

$$Gain_{MAX} = Available\ Output\ Swing/Input\ Range$$

Also for bipolar inputs (that is, input range = 2 V_{DIFF}), the maximum gain is half the value yielded by the previous equations because the REF pin must be at midsupply.

The maximum gain and resulting output swing for different input conditions is given in Table 10. Output voltages are referenced to the voltage on the REF pin.

For the purposes of computation, it is necessary to break down the input voltage into its differential and common-mode components. Therefore, when one of the inputs is grounded or at a fixed voltage, the common-mode voltage changes as the differential voltage changes. Take the case of the thermocouple amplifier in Figure 54. The inverting input on the AD623 is grounded; therefore, when the input voltage is −10 mV, the voltage on the noninverting input is −10 mV. For the purpose of the signal swing calculations, this input voltage must be composed of a common-mode voltage of −5 mV (that is, (+IN + −IN)/2) and a differential input voltage of −10 mV (that is, +IN − −IN).

Table 10. Maximum Attainable Gain and Resulting Output Swing for Different Input Conditions

V_{CM}	V_{DIFF}	REF Pin	Supply Voltages	Maximum Gain	Closest 1% Gain Resistor	Resulting Gain	Output Swing
0 V	±10 mV	2.5 V	+5 V	118	866 Ω	116	±1.2 V
0 V	±100 mV	2.5 V	+5 V	11.8	9.31 kΩ	11.7	±1.1 V
0 V	±10 mV	0 V	±5 V	490	205 Ω	488	±4.8 V
0 V	±100 mV	0 V	±5 V	49	2.1 kΩ	48.61	±4.8 V
0 V	±1 V	0 V	±5 V	4.9	26.1 kΩ	4.83	±4.8 V
2.5 V	±10 mV	2.5 V	+5 V	242	422 Ω	238	±2.3 V
2.5 V	±100 mV	2.5 V	+5 V	24.2	4.32 kΩ	24.1	±2.4 V
2.5 V	±1 V	2.5 V	+5 V	2.42	71.5 kΩ	2.4	±2.4 V
1.5 V	±10 mV	1.5 V	+3 V	142	715 Ω	141	±1.4 V
1.5 V	±100 mV	1.5 V	+3 V	14.2	7.68 kΩ	14	±1.4 V
0 V	±10 mV	1.5 V	+3 V	118	866 Ω	116	±1.1 V
0 V	±100 mV	1.5 V	+3 V	11.8	9.31 kΩ	11.74	±1.1 V

ADDITIONAL INFORMATION

For an updated design of the AD623, see the AD8223.

For a selection guide to all Analog Devices instrumentation amplifiers, see the Instrumentation Amplifiers page on the Analog Devices website at www.analog.com.

For additional information on in-amps, refer to the following:

MT-061. *Instrumentation Amplifier (In-Amp) Basics.* Analog Devices, Inc.

MT-070. *In-Amp Input RFI Protection.* Analog Devices, Inc.

Counts, Lew and Charles Kitchen. *A Designer's Guide to Instrumentation Amplifiers.* 3rd edition. Analog Devices, Inc., 2006.

EVALUATION BOARD

GENERAL DESCRIPTION

The EVAL-INAMP-62RZ can be used to evaluate the AD620, AD621, AD622, AD623, AD627, AD8223, and AD8225 instrumentation amplifiers. In addition to the basic in-amp connection, circuit options enable the user to adjust the offset voltage, apply an output reference, or provide shield drivers with user supplied components. The board is shipped with an assortment of instrumentation amplifier ICs in the legacy SOIC pinout, such as the AD620, AD621, AD622, AD623, AD8223, and AD8225. The board also has an alternative footprint for a through-hole, 8-lead PDIP.

Figure 56 shows a photograph of the evaluation boards for all Analog Devices instrumentation amplifiers. For additional information, see the EVAL-INAMP user guide (UG-261).

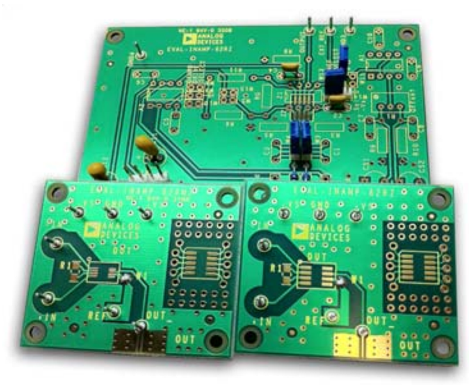
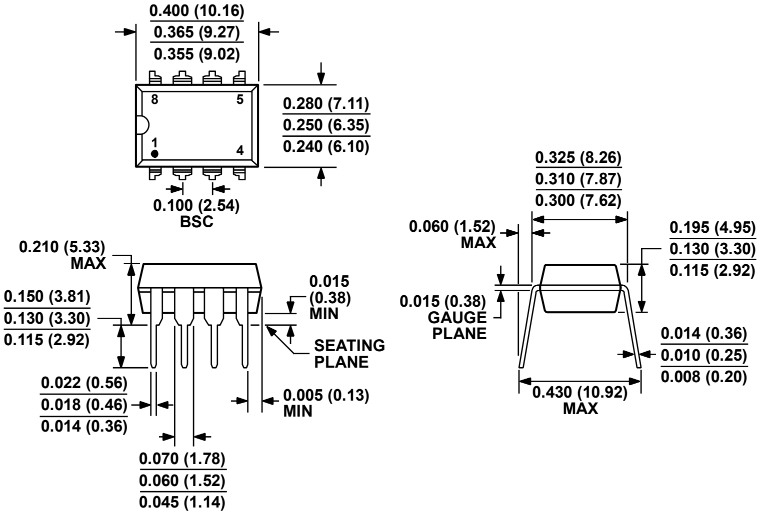


Figure 56. Evaluation Boards for Analog Devices In-Amps

OUTLINE DIMENSIONS

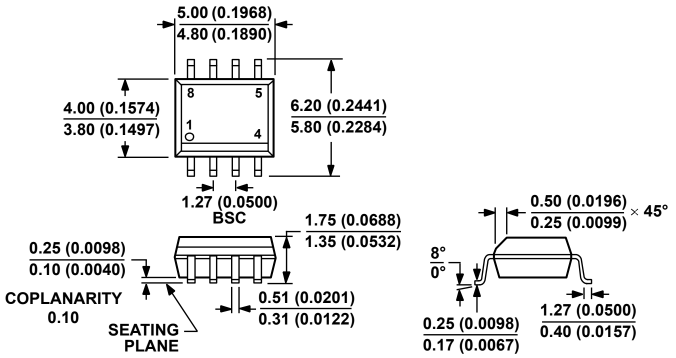


COMPLIANT TO JEDEC STANDARDS MS-001

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 57. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body (N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 58. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

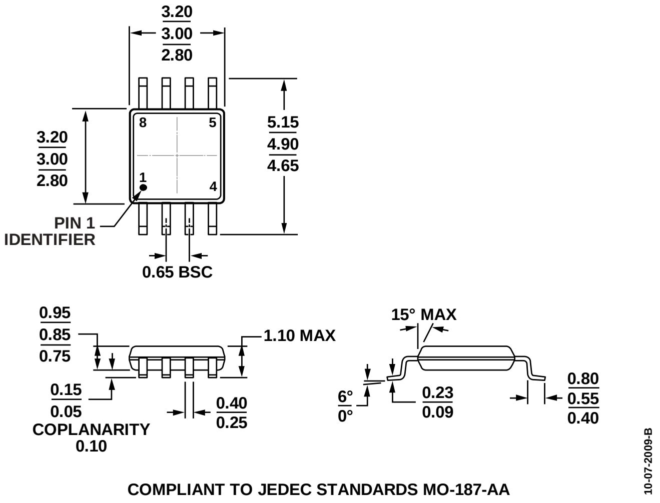


Figure 59. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD623ANZ	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8	
AD623AR	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD623AR-REEL7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N], 7" Tape and Reel	R-8	
AD623ARZ	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD623ARZ-R7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N], 7" Tape and Reel	R-8	
AD623ARZ-RL	−40°C to +85°C	8-Lead SOIC, 13" Tape and Reel	R-8	
AD623ARMZ	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	J0A
AD623ARMZ-REEL	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP], 13" Tape and Reel	RM-8	J0A
AD623ARMZ-REEL7	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP], 7" Tape and Reel	RM-8	J0A
AD623BNZ	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8	
AD623BRZ	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD623BRZ-R7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N], 7" Tape and Reel	R-8	
AD623BRZ-RL	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N], 13" Tape and Reel	R-8	
EVAL-INAMP-62RZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

TL081

TL081 Wide Bandwidth JFET Input Operational Amplifier

Literature Number: SNOSBW6A

National Semiconductor

December 1995

TL081 Wide Bandwidth JFET Input Operational Amplifier

General Description

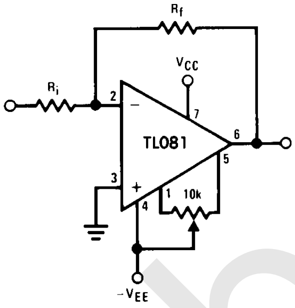
The TL081 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL081 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The TL081 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the TL081C is the better choice.

Features

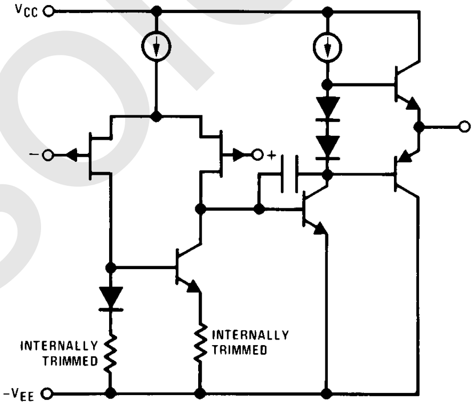
■ Internally trimmed offset voltage	15 mV
■ Low input bias current	50 pA
■ Low input noise voltage	25 $nV/\sqrt{Hz}$
■ Low input noise current	0.01 $pA/\sqrt{Hz}$
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz−20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



TL/H/8358–1

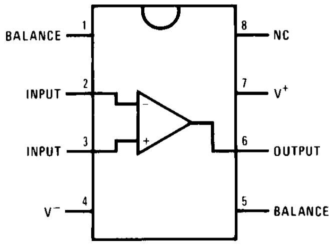
Simplified Schematic



TL/H/8358–2

Connection Diagram

Dual-In-Line Package



TL/H/8358–4

Order Number TL081CP
See NS Package Number N08E

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Notes 1 and 6)	670 mW
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C
θ_{jA}	120°C/W

ESD rating to be determined.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	TL081C			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C Over Temperature		5	15 20	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10		μV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 3, 4) T_j ≤ 70°C		25	100 4	pA nA
I_B	Input Bias Current	T_j = 25°C, (Notes 3, 4) T_j ≤ 70°C		50	200 8	pA nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C V_O = ±10V, R_L = 2 kΩ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	R_S ≤ 10 kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	70	100		dB
I_S	Supply Current			1.8	2.8	mA

AC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	TL081C			Units
			Min	Typ	Max	
SR	Slew Rate	V_S = ±15V, T_A = 25°C		13		V/μs
GBW	Gain Bandwidth Product	V_S = ±15V, T_A = 25°C		4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 120°C/W junction to ambient for N package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

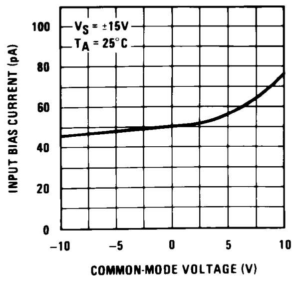
Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from V_S = ±5V to ±15V.

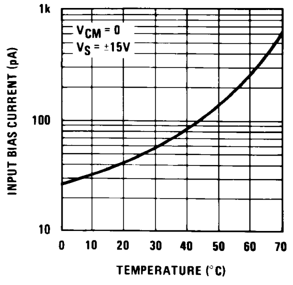
Note 6: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

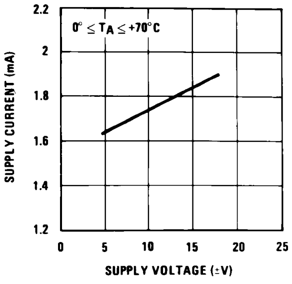
Input Bias Current



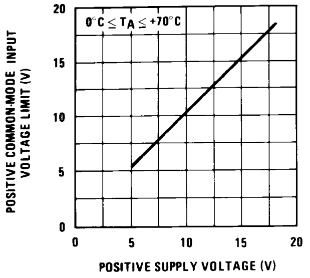
Input Bias Current



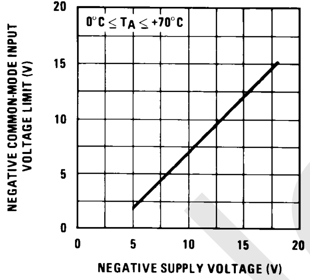
Supply Current



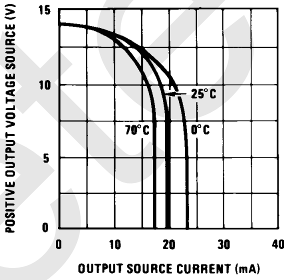
Positive Common-Mode Input Voltage Limit



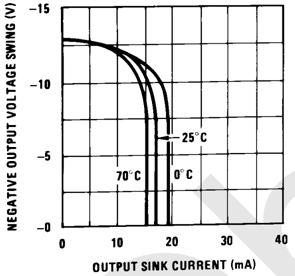
Negative Common-Mode Input Voltage Limit



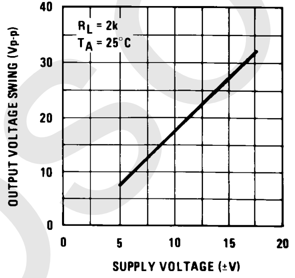
Positive Current Limit



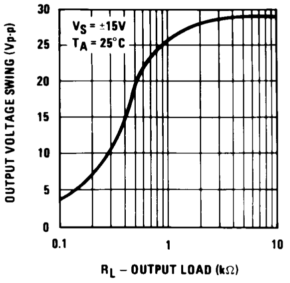
Negative Current Limit



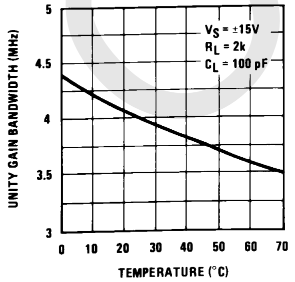
Voltage Swing



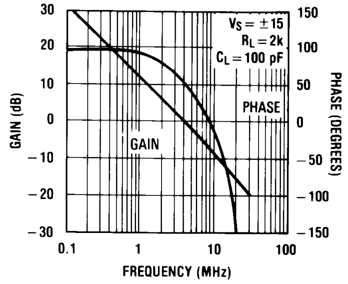
Output Voltage Swing



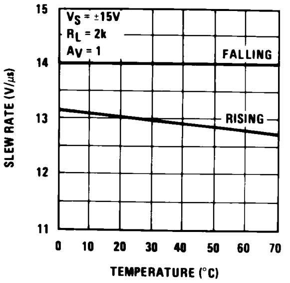
Gain Bandwidth



Bode Plot

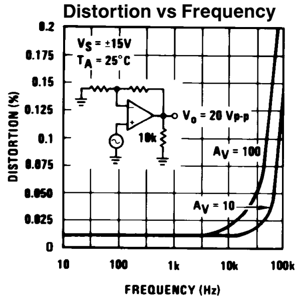


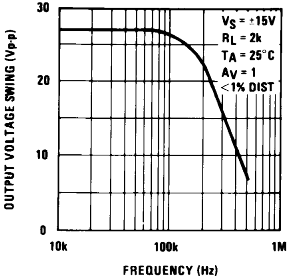
Slew Rate

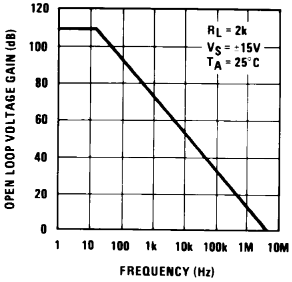


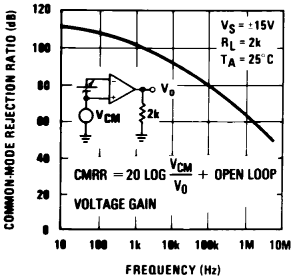
TL/H/8358–5

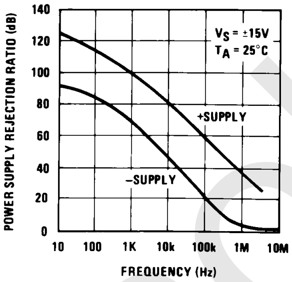
Typical Performance Characteristics (Continued)

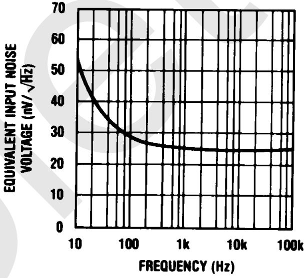

Distortion vs Frequency

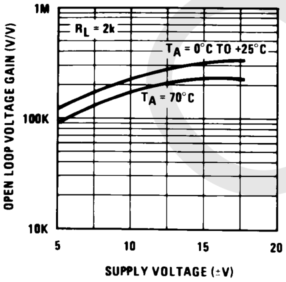

Undistorted Output Voltage Swing

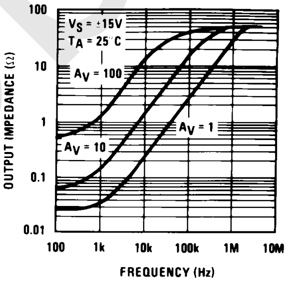

Open Loop Frequency Response

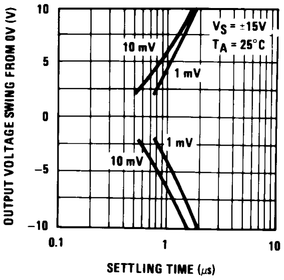

Common-Mode Rejection Ratio


Power Supply Rejection Ratio


Equivalent Input Noise Voltage


Open Loop Voltage Gain (V/V)

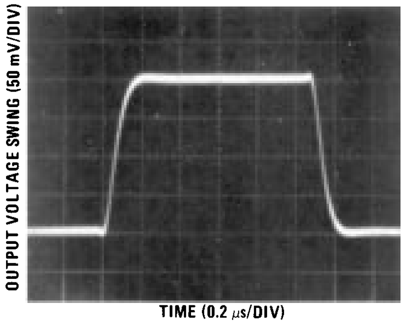

Output Impedance


Inverter Settling Time

TL/H/8358–6

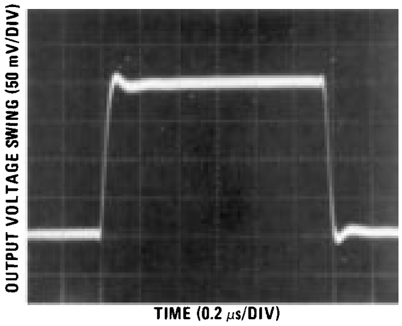
Pulse Response

Small Signal Inverting



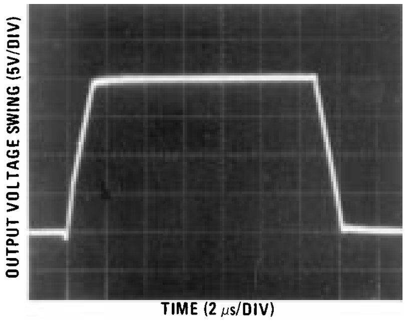
TL/H/8358–7

Small Signal Non-Inverting



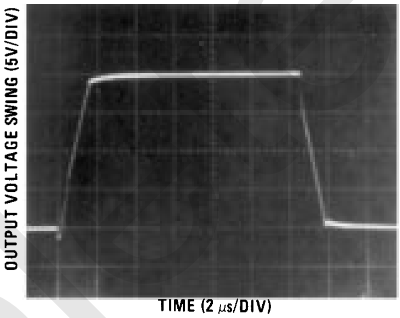
TL/H/8358–13

Large Signal Inverting



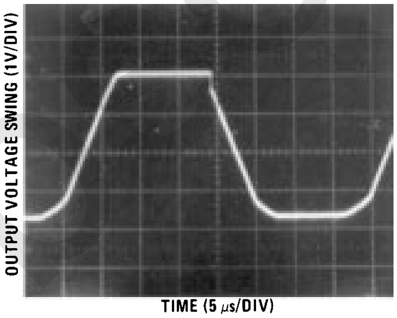
TL/H/8358–14

Large Signal Non-Inverting



TL/H/8358–15

Current Limit ($R_L = 100\Omega$)



TL/H/8358–16

Application Hints

The TL081 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the

Application Hints (Continued)

common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The TL081 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The TL081 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

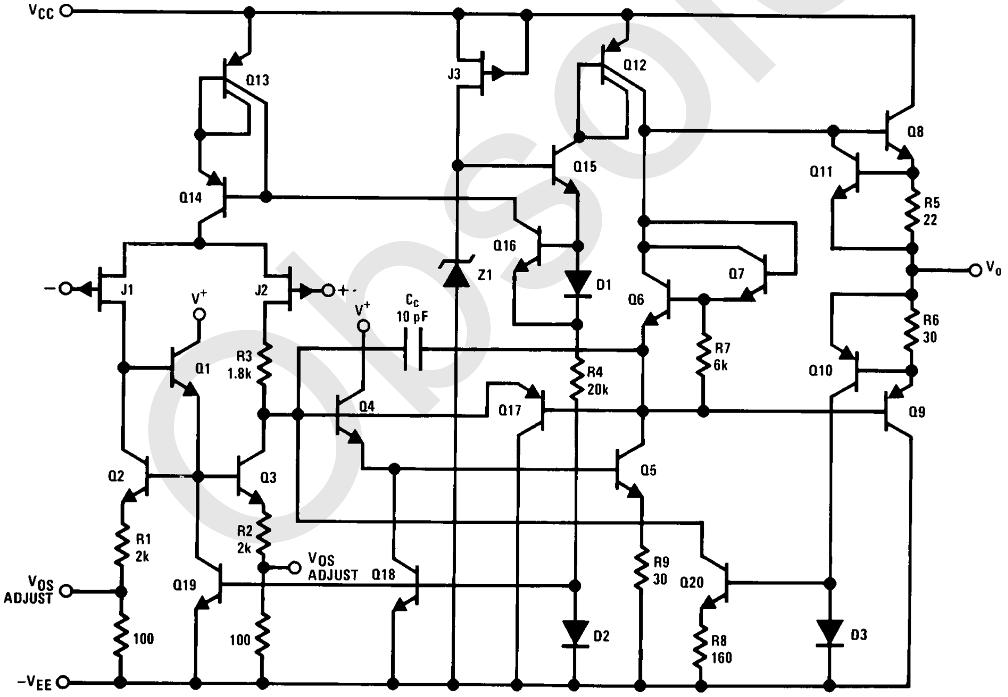
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

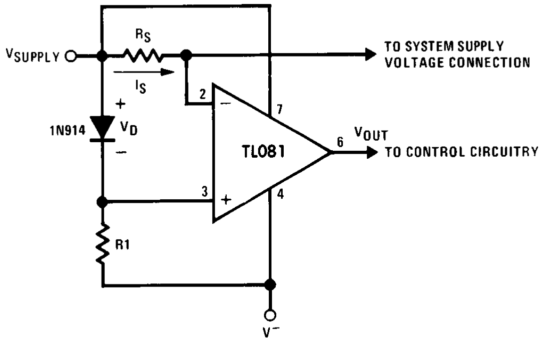
Detailed Schematic



TL/H/8358–8

Typical Applications

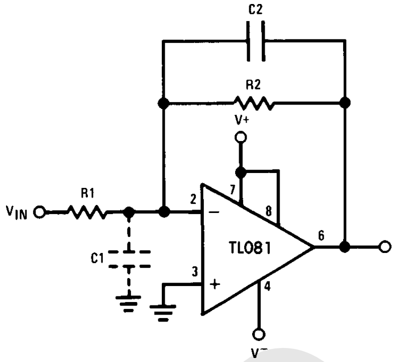
Supply Current Indicator/Limiter



TL/H/8358–9

- V_{OUT} switches high when $R_S I_S > V_D$

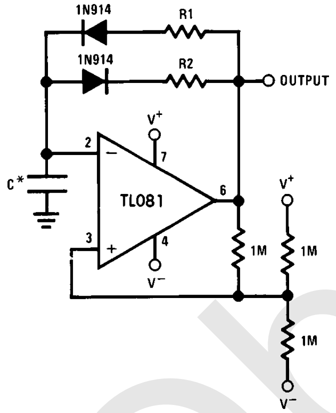
Hi-Z_{IN} Inverting Amplifier



TL/H/8358–10

Parasitic input capacitance C1 ≅ (3 pF for TL081 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

Ultra-Low (or High) Duty Cycle Pulse Generator



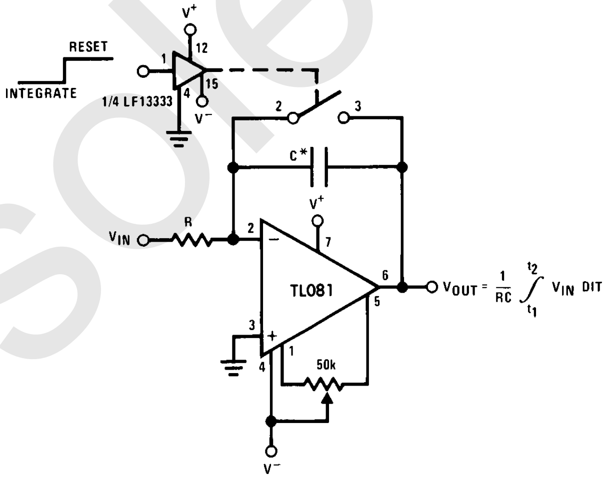
TL/H/8358–11

- $t_{OUTPUT\ HIGH} \approx R1C\ \ell n \dfrac{4.8 - 2V_S}{4.8 - V_S}$
- $t_{OUTPUT\ LOW} \approx R2C\ \ell n \dfrac{2V_S - 7.8}{V_S - 7.8}$

  where $V_S = V^+ + |V^-|$

*low leakage capacitor

Long Time Integrator

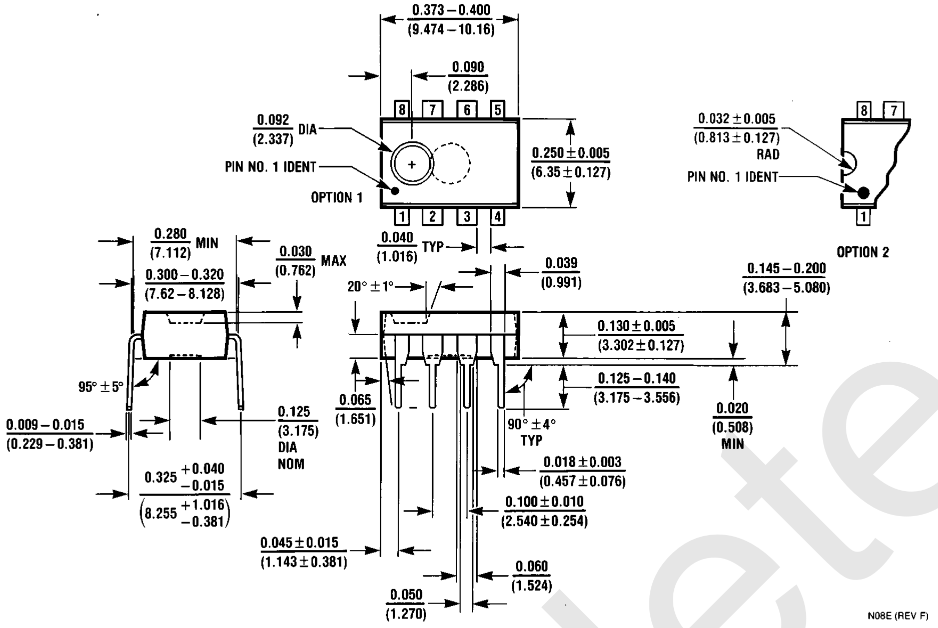


TL/H/8358–12

* Low leakage capacitor

- 50k pot used for less sensitive V_{OS} adjust

Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number TL081CP
NS Package Number N08E

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