Abstract

ALICE (A Large Ion Collider Experiment) is the heavy-ion experiment at the Large Hadron Collider (LHC) at CERN. As an important part of its upgrade plans, the ALICE experiment will schedule the installation of a new Inner Tracking System (ITS) during the Long Shutdown 2 (LS2) of the LHC. The new ITS layout will consist of seven concentric layers, $\approx$ 12.5 Gigapixel camera covering about 10m^2 with Monolithic Active Pixel Sensors (MAPS). This choice of technology has been guided by the tight requirements on the material budget of 0.3% X/X_0 per layer for the three innermost layers and backed by the significant progress in the field of MAPS in recent years. The technology initially chosen for the ITS upgrade is the TowerJazz 180 nm CMOS Technology. It offers a standard epitaxial layer of 15 - 18 μm with a resistivity between 1 and 5 kΩ cm^{-1} and a gate oxide thickness below 4 nm, thus being more robust to Total Ionizing Dose (TID).

The main subject of this thesis is to implement a novel digital pixel readout architecture for MAPS. This thesis aims to study this novel readout architecture as an alternative to the rolling-shutter readout. However, this must be investigated through the study of several chip readout architectures during the R&D phase. Another objective of this thesis is the study and characterization of TowerJazz, if it meets the Non-Ionizing Energy Loss (NIEL) and Single Event Effects (SEE) of the ALICE ITS upgrade program.

Other goals of this thesis are:

- Implementation of the top-down flow for this CMOS process and the design of multiple readouts for different prototypes up to the assembly of a full-scale prototype.

- Characterization of the radiation hardness and SEE of the chips submitted to fabrication.
- Characterization of full custom designs using analog simulations and the generation of digital models for the simulation chain needed for the verification process.
- Implementation and study of different digital readouts to meet the ITS upgrade program in integration time, pixel size and power consumption, from the conceptual idea, production and fabrication phase.

Chapter 1 is a brief overview of CERN, the LHC and the detectors complex. The ALICE ITS will be explained, focusing on the ITS upgrade in terms of detector needs and design constraints. Chapter 2 explains the properties of silicon detectors and the detector material and the principles of operation for MAPS. Chapters 3 and 4 describe the ALPIDE prototypes and their readout based on MAPS; this forms the central part of this work, including the multiple families of pixel detectors fabricated in order to reach the final design for the ITS. The ALPIDE3/pALPIDE3B chip, the latest MAPS chip designed, will be explained in detail, as well focusing in the matrix digital readout. In chapter 5 the noise measurements and its characterization are presented including a brief summary of detector response to irradiation with soft X-rays, sources and particle beams.