Readout and Data Acquisition in the NEXT-NEW Detector based on SRS-ATCA

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ABSTRACT:

The Scalable Readout System (SRS) was defined by the CERN RD51 Collaboration as a multi-channel, scalable readout platform for a wide range of front ends. In 2014, SRS was ported to the ATCA (Advanced Telecommunications Computing Architecture) standard.

NEXT is an underground experiment aimed at searching for neutrinoless double-beta decay. NEXT-DEMO, a small-scale demonstrator, was read-out using SRS. NEXT has adopted SRS-ATCA for its first stage, called NEXT-NEW. Our presentation will describe the readout, DAQ and trigger for NEXT-NEW based on SRS-ATCA. This is, to our knowledge, the first experiment operating entirely on SRS-ATCA.

KEYWORDS: Data acquisition circuits, FPGA, ATCA.

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Contents

1. Introduction

1.1 ATCA in high-energy and nuclear physics

ATCA (Advanced Telecom Computing Architecture) is a PICMG 3.x standard that provides a reliable and scalable switched-based architecture to build data acquisition (DAQ) and trigger systems. It allows large-enough modules (7.25 U x 230 mm), adequate power consumption (cooling is designed for at least 200 W per module) and large interconnection bandwidth (the majority of recent implementations use 10 Gb/s channels, each consisting of four differential pairs) for today's high-energy and nuclear physics experiments. A brief discussion of the ATCA standard and its potential application to real-time systems is presented in [1]. More specifically, its suitability for the LHC DAQ upgrade was pointed out in [2].

Most ATCA implementations define FPGA-based processing carrier boards that accept I/O from several mezzanine boards in the front panel. These contain transceivers, frequently FPGAs and fast memories in some cases. Additionally, each carrier module can have an optional rear transition module (RTM) to provide additional I/O from the rear of the chassis. Boards are interconnected via high-speed serial backplanes implementing either a star topology (one slot in the chassis acts as a switch and each of the other modules provides a 4-pair channel to it), or more frequently, a full mesh (all slots provide one channel to every other slot). Neighbouring modules have dedicated interconnection channels in the backplane.

Among other features, ATCA chassis provide clocking, shelf management, hot swap capabilities and optional redundant cooling and power supplies. ATCA modules communicate with the shelf manager using the Intelligent Platform Management Interface (IPMI). This is known to be complex to implement, posing a non-negligible overhead and usually requiring a dedicated microcontroller.

Two representative examples of the current trend are described below. The first example is the Computing Node for the Belle II pixel detector DAQ and data reduction system [3]. In one of the two board versions, an ATCA carrier module accommodates 4 AMC mezzanines, each housing an FPGA, DDR2 memory, two SFP optical links (input data flow) and a Gbit Ethernet connector (output data flow). The carrier board provides a full-mesh interconnection (using $\leq$

6.5 Gb/s transceivers) between the four FPGAs in the mezzanines and a fifth FPGA in the carrier board, the latter being responsible to communicate with a full-mesh backplane in the ATCA chassis.

The second example is the Pulsar II ATCA carrier board [4] developed for the ATLAS Fast Tracker Data Formatter system, a trigger application. The full-mesh connectivity in the ATCA backplane is used to transfer time multiplexed event data from input boards to multiple track processing engines. The carrier board accommodates four mezzanine cards and two processing FPGAs (only one in the later Pulsar IIb revision), each with a dedicated DDR3 memory. The FPGAs directly interface the backplane using its embedded 10 Gb/s transceivers instead of a dedicated switch IC, thus allowing custom efficient protocols (this solution is also found in [3]). A RTM provides expanded I/O via 14 pluggable QSFP+ and SFP+ transceivers for an aggregate bandwidth of 380 Gbps.

In both cases, as in many others, multi-gigabit full-mesh connectivity was key to the choice of ATCA as DAQ/trigger architecture.

1.2 The Scalable Readout System (SRS)

The Scalable Readout System (SRS) is an IP co-owned by CERN, Universitat Politècnica de València and IFIN-HH Bucharest. It was defined by the CERN RD51 Collaboration [5-6] as a scalable, multi-channel readout platform intended for small set-ups and medium-scale experiments. It was first conceived in 2009 with micro-pattern gaseous detectors in mind, though its flexibility allows targeting any kind of front-end. SRS has two main building blocks:

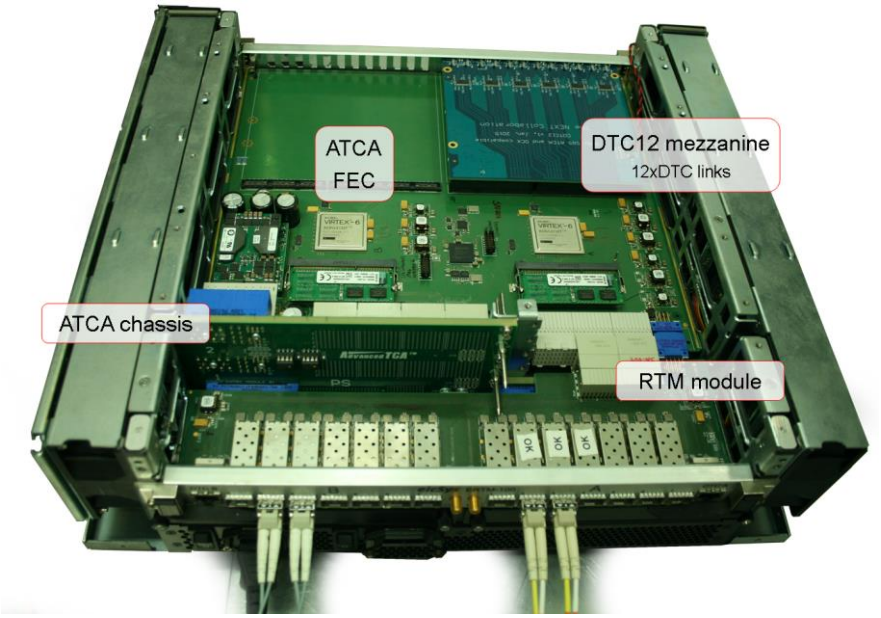
1. The Front-End Concentrator card (FEC) [7] is a flexible front-end interface and data concentrator. This 6U-height FPGA-based card processes data coming from edge-mounted add-in cards. A variety of add-in cards exist with ADC channels, LVDS interfaces, or more specific front-ends like APV25, Beetle, VFAT or VMM2 ASICs. In the front panel, a number of connectors provide power, two SFP+ transceivers (usually Gbit Ethernet), NIM I/O and auxiliary RJ-45 sockets. The later allow implementing custom links [8] named DTCC carrying clock, slow controls, trigger and data over copper.
2. The Scalable Readout Unit (SRU) is a second data concentrator stage intended for larger scale applications.

Both modules are based on FPGA and can interface a DAQ PC farm via GbE links, thus reducing the DAQ and trigger systems to a network-based architecture. Many research institutions worldwide have successfully used SRS, including our first detector prototype (NEXT-DEMO) [9].

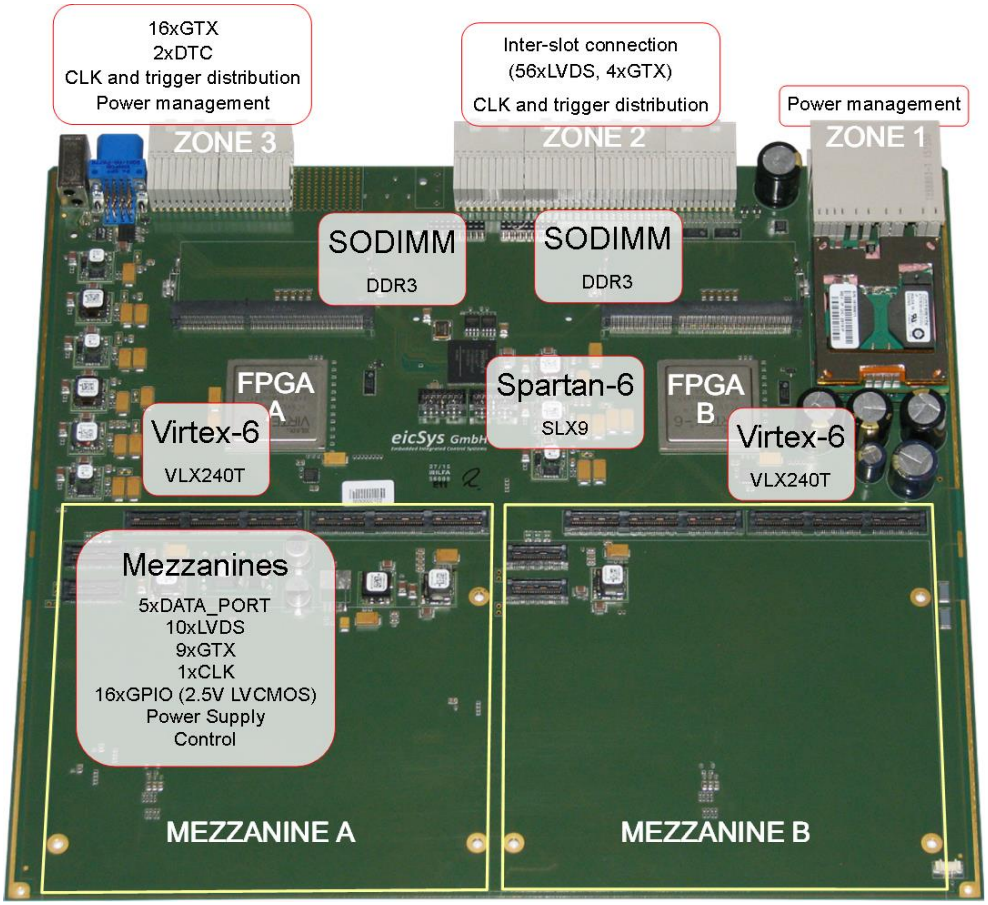
2. SRS-ATCA implementation

In 2014, SRS was ported to the ATCA (Advanced Telecommunications Computing Architecture) standard upon agreement with the German company EicSys. The use of certified crates with built-in and redundant cooling, power and shelf management makes it a more robust mechanical and electrical solution for prolonged operation in experiments than the original SRS flavour based on light Eurocard crates. Higher data bandwidth is achieved by replacing the DTCC link cables with multi-gigabit channels across a full-mesh backplane, enabling 10 Gb/s I/O through the RTM and using faster FPGA and memory.

Figure 1 shows a picture of the 2-slot ACTA chassis provided by EicSys that has been used in the first tests of the NEXT-NEW experiment.



101 **Figure 1.** A two-slot ATCA chassis used in initial tests.



102 **Figure 2.** ATCA FEC module (2015 version).

The ATCA-FEC carrier (figure 2) has two Xilinx Virtex-6 FPGAs (XC6VLX240T-1ff1156) and a DDR3 SO-DIMM memory module for each FPGA. The two FPGAs are interconnected via high-speed links. A third FPGA, a Spartan-6, is used for board management purposes. Two on-board custom mezzanine connectors provide I/O flexibility for a wide range of front ends. Two mezzanine models exist with 24 ADC channels (12 bit, up to 60 MSa/s) and 12 DTCC links on HDMI connectors to interface digital front ends. In-design mezzanines include multi-gigabit optical transceivers with FPGAs. The ATCA-FEC is functionally equivalent to 2 "classic" FEC modules. SRS-ATCA includes rear transition modules (RTM) for multiple GbE, 10 GbE and other I/O connectivity. ATCA backplanes exist with full mesh and star topologies, using 10 Gb/s channels.

Besides NEXT-NEW, another application for SRS-ATCA is the micromegas detector readout for the upgrade of the ATLAS muon spectrometer [10].

3. DAQ and trigger requirements in the NEXT-NEW detector

NEXT [11] is an underground experiment aimed at searching for neutrinoless double-beta decay that combines an excellent energy resolution with tracking capabilities merging PMTs and SiPMs. NEXT-DEMO, a small-scale demonstrator, was read out using classical SRS. NEXT has adopted SRS-ATCA for its first stage, called NEXT-NEW. This detector (figure 3) is a half scale of the final detector and it will be installed in the Canfranc Underground Laboratory (LSC) using the same platform, gas system and external shielding.

Figure 3. The NEW detector at Canfranc Underground Laboratory (LSC).

The detector is a time-projection chamber filled with 10 kg of ^{136}Xe gas at 15 bar. Electrons from double-beta decays will drift towards the anode end cap under the effect of an electric field, ionizing other atoms in their movement. Close to the anode, electrons are further accelerated by an additional electric field to produce electroluminescence.

Light received in an array of 1,800 SiPMs in the anode (tracking plane) is used to reconstruct electron tracks in order to reject background events. SiPM sensors are laid out with a 1-cm pitch and grouped in twenty-eight 8x8 arrays. Front-end boards [12] integrate and digitize (12 bit, 1 MSa/s) 64 channels, resulting in approx. 1 Mb of data per event per front-end

board, taking into account the framing overhead. For 28 front-end boards, 1 ms events and a 10 Hz trigger rate, the SiPM tracking partition generates 35 MByte/s in raw data mode.

Light produced by electroluminescence is reflected to the energy plane in the cathode end cap where and array of 12 PMTs is used to measure the energy of the event with a resolution better than 1%. PMTs also sense the initial scintillation light produced in the double-beta decay, giving a timestamp and a z-coordinate for the event. PMT signals are digitized at 40 MSa/s, 12 bit. Once digitized and framed, this produces approximately 10 MByte/s for the 12 PMTs at a 10 Hz rate.

Dead time must be minimized, suggesting the use of double buffers. These are implemented in the SiPM front-end boards for the tracking plane partition, and in the ATCA-FEC's DDR3 memory in the case of the energy plane partition. Events are configurable in length up to 3.2 ms, with a nominal value of 1.6 ms. NEXT-NEW is expected to operate at a 10 Hz trigger rate produced by background events.

Three different DAQ modes must be supported: (1) raw data mode, (2) Normal Mode 1 ("normal events" are sent zero-suppressed, and "interesting events" are sent in raw mode) and (3) Normal Mode 2 (similar to Normal Mode 1, but the double buffer –and thus the dead time reduction- is only used for "interesting events").

The trigger algorithm [13] must combine information from the first scintillation light as well as from the early total event energy estimation. A trigger is generated if (1) a defined number of PMTs have detected at least a certain number of scintillation photons within a defined time window, and (2) some time after the scintillation, the estimated total integrated energy in a defined time window is within certain upper and lower bounds. All thresholds and levels must be configurable. The trigger algorithm must be implemented on FPGA.

4. Readout and DAQ Architecture for NEXT-NEW

Reading out the 28 SiPM front-end boards in the tracking plane partition requires one and a half ATCA-FECs and a total of three digital interface mezzanines (each one having 12 DTCC interfaces over HDMI). Front-end boards work in free-running mode, storing data continuously in a circular buffer. Data are only sent to the ATCA-FEC modules when a timestamped trigger is received.

The energy plane (12 PMTs) is read out with a single 24-channel ADC mezzanine plugged onto half ATCA-FEC module, which sends trigger candidates based on early energy estimations to another half ATCA-FEC (used as trigger module). As a result, three ATCA-FECs are needed to read out the detector's energy and tracking planes and implement the trigger algorithm. Each ATCA-FEC interfaces a DAQ PC via 4 Gigabit Ethernet optical links.

Communication between the trigger module (half ATCA-FEC) and the other DAQ modules should normally make use of high-speed channels in the backplane, be it star or full mesh (both are valid for our application). Implementing the DTCC functionalities in these channels would efficiently address clock, trigger, slow controls and data (trigger candidates) distribution. In an initial stage of operation, in order to ease the porting of the firmware from "classical" SRS to SRS-ATCA, a digital interface mezzanine will be used to create DTCC links over HDMI, which connect to DTCC HDMI sockets in the RTMs in the ATCA-FECs. This mimics the solution used in NEXT-DEMO. A NIM input in the RTM module allows external triggers if needed.

The DAQ PC farm comprises three local data concentrator PCs (each connected to an ATCA-FEC via 4 Gigabit Ethernet optical links), two global data concentrator PCs (for event

buiding) and a storage PC (equipping a number of hard disks). A Gigabit Ethernet switch interconnects these six PCs. A complete scheme of the NEXT-NEW DAQ and trigger system is shown in figure 4.

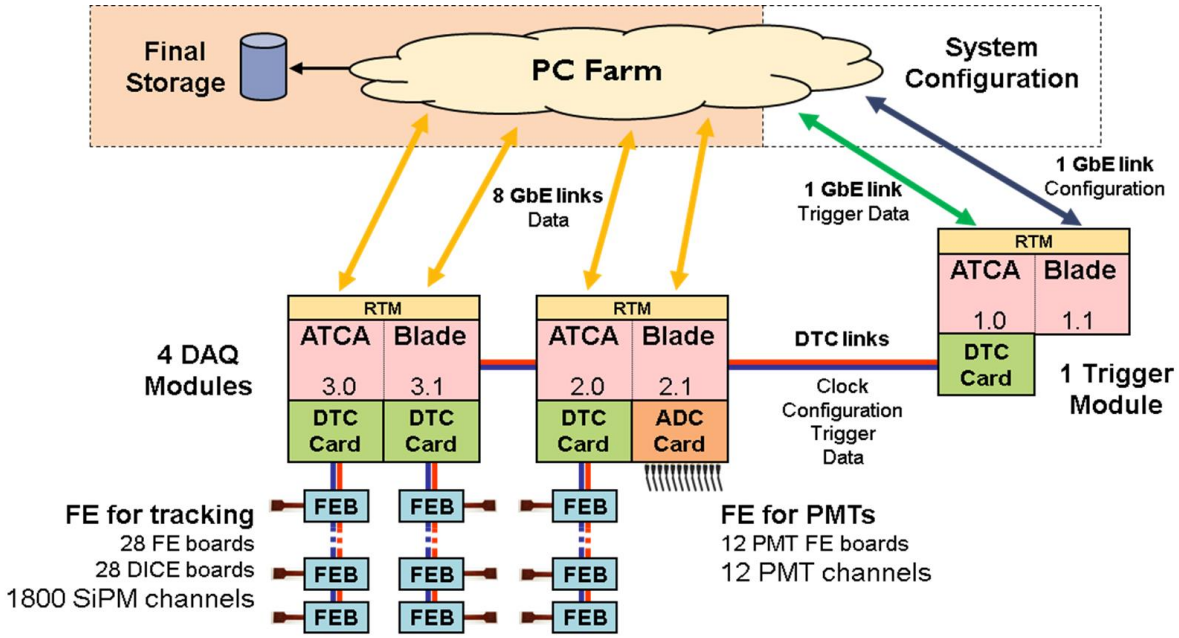


Figure 4. NEXT-NEW DAQ and trigger system architecture.

In a first step, the NEXT-NEW detector, readout and DAQ system, only for the energy plane, was installed and tested at the Canfranc Underground Laboratory during September 2015 (see figure 5). The complete system described in figure 4 has been already successfully validated in laboratory. Installation and initial operation with the NEXT-NEW detector in the Canfranc Underground Laboratory (LSC) is scheduled for November 2015.

5. Conclusions

SRS, in its "classic" flavour, is a successful DAQ and trigger solution for our first prototype NEXT-DEMO as well as for many other applications in the CERN RD51 community. Long-term operation of NEXT-NEW and the final NEXT detector in an underground laboratory poses more stringent demands on reliability and performance. Porting SRS to the ATCA standard, using the same key technologies (same FPGAs, functional blocks and protocols), provides an adequate upgrade for the hardware with the additional benefit of an easy migration path for the firmware.

The complete readout, DAQ and trigger system has been validated in laboratory prior to installation in the underground laboratory in November 2015. As early users, we had access to a beta version of the ATCA-FEC module and helped to identify minor design bugs in the course of our tests. NEXT-NEW is, to our knowledge, the first experiment operating entirely on SRS-ATCA.

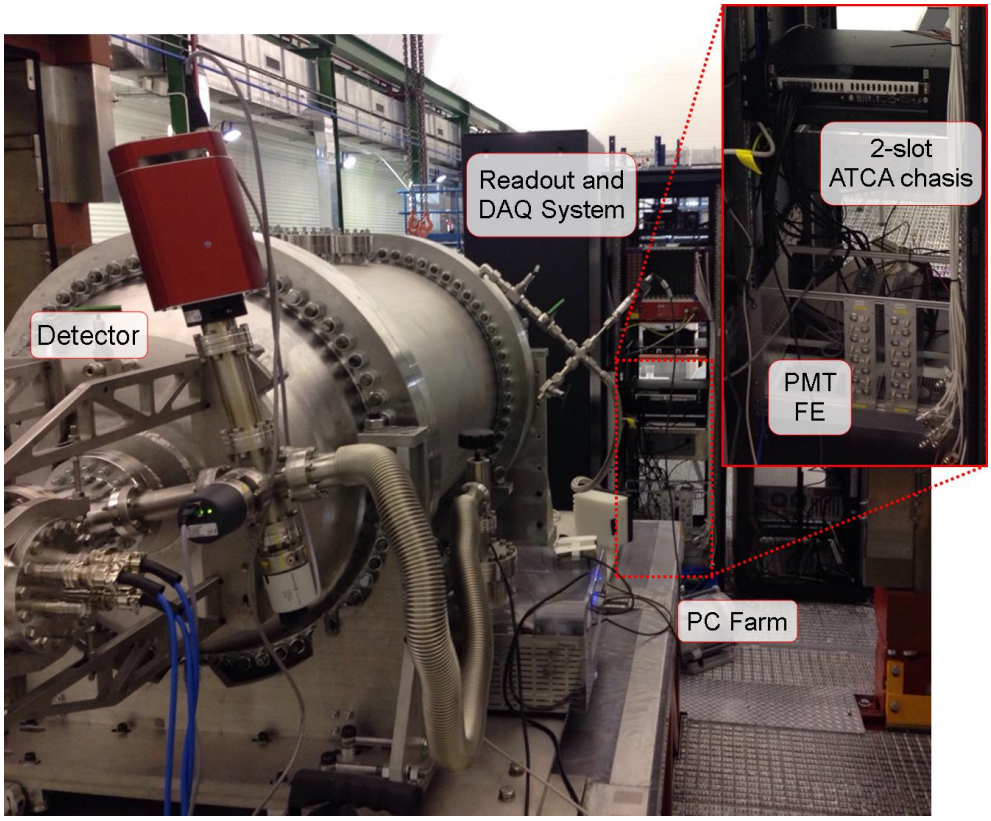


Figure 5. NEXT-NEW detector, readout and DAQ system installation in the Canfranc Underground Laboratory.

Acknowledgments

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